White Paper

Improving Fidelity of Noise Repetitive Signals with Signal Averaging Technology

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Abstract

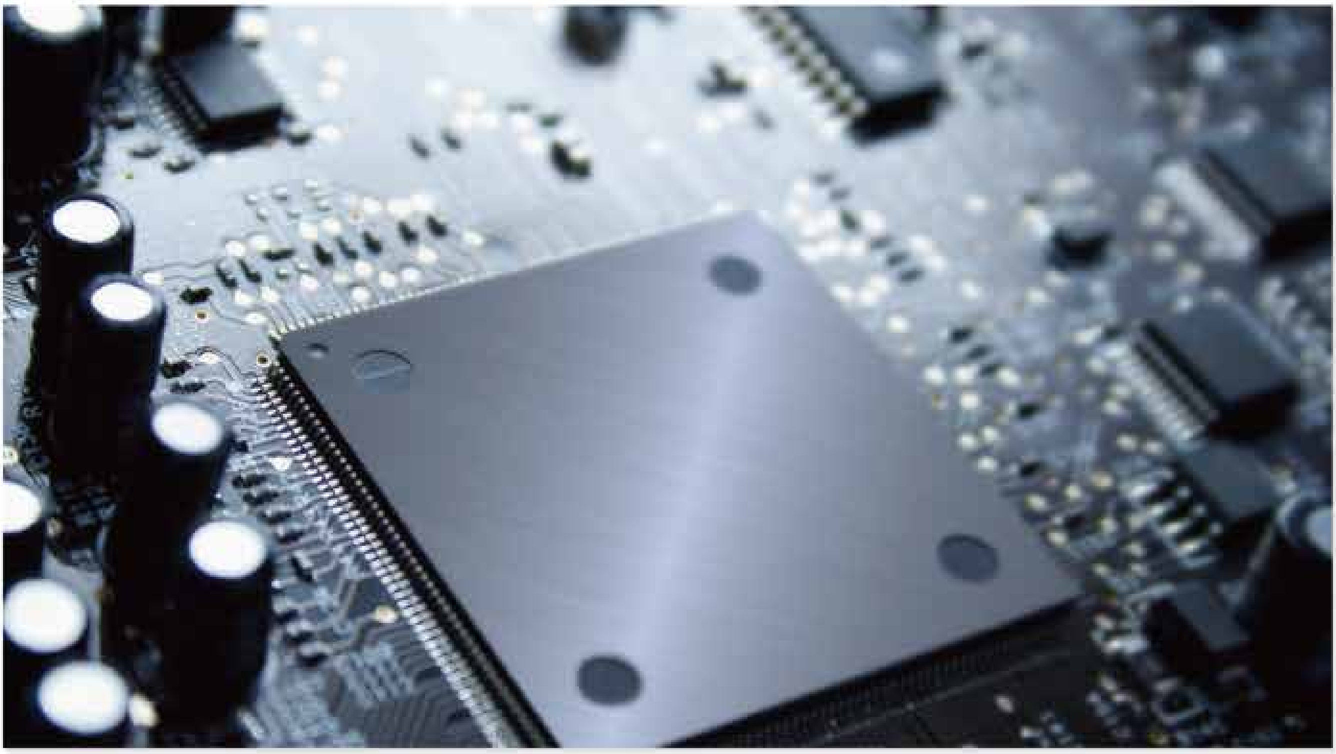
For many high-speed data acquisition applications requiring extraction of small repetitive signals from noisy environments, such as LIDAR or optical fiber testing, minimizing the effects of noise is a challenge for system design. Signal averaging provides dependable and efficient results.

Often, during measurement of analog signals, captured data can carry unwanted random additional content, generated by surrounding disturbances or observation errors, most often manifesting as random noise that may obscure the target signal. Signal averaging processes signals so as to reduce noise effects, improve the signal-to-noise ratio (SNR), while improving resolution and dynamic range. In particular, ADLINK's Data Average Mode delivers a superior level of function when signal averaging is indicated.

The FPGA Advantage

Elimination of noise from captured data can be accomplished by either DSP- or FPGA-based solutions. If the system sampling rate is below a few kilohertz, the DSP solution can be employed. When the sampling rate is higher, however, the FPGA (field-programmable gate array) is preferable, since the DSP is code or instruction based such that the process inevitably involves architecture and core processing, all of which occupies resources and processing time. Alternatively, the FPGA provides multiple gates and ram block to form multipliers, registers, and other measures, rendering it capable of implementing prompt calculations. In many currently popular high performance applications, DSPs can struggle, making FPGA-based solutions more frequently chosen.

Many of ADLINK's high-speed digitizers feature onboard FPGA addressing real-time applications requiring speedy sampling and high bandwidth. The FPGA board also allows off-board real-time data processing capabilities such as signal averaging, relieving the system host of any signal averaging duties. Signal averaging is accomplished much faster than on the host, with no usage whatever of the host CPU.



Improving the fidelity of noise repetitive signals

When measuring analog signals, captured data contains some measure of noise that may obscure the signal of interest or, for example, its harmonic content, modulation sidebands, and so on. As is known, expected mean values of random noise are zero, making signal averaging a simple and effective way to rid target data of random noise in periodic or repeating signals. Data Average Mode on the PCIe/PXIe-9852 is implemented as follows. In repeat acquisition of N samples R times in re-trigger mode, with trigger sources external digital or analog, each acquisition is stored in the same onboard buffer and accumulated automatically by a FPGA with no software intervention. When the R times retrigger is complete, the FPGA divides the accumulated data by R and transfers to the host PC. The data comprises the average of R traces sample by sample, with noise reduced, closer to the target data. Characteristics of signal acquisition and noise reduction in the PCIe/PXIe-9852 Data Average Mode are as shown.

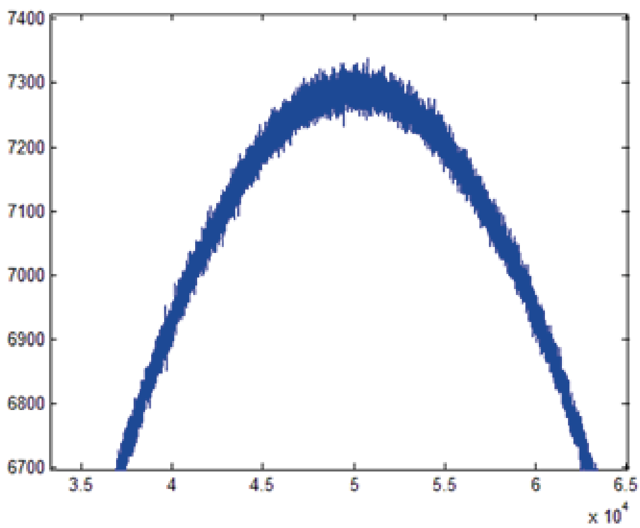


Fig1. Single Acquisition of a 1k Hz, 3.6vpp Sine Wave with Noise

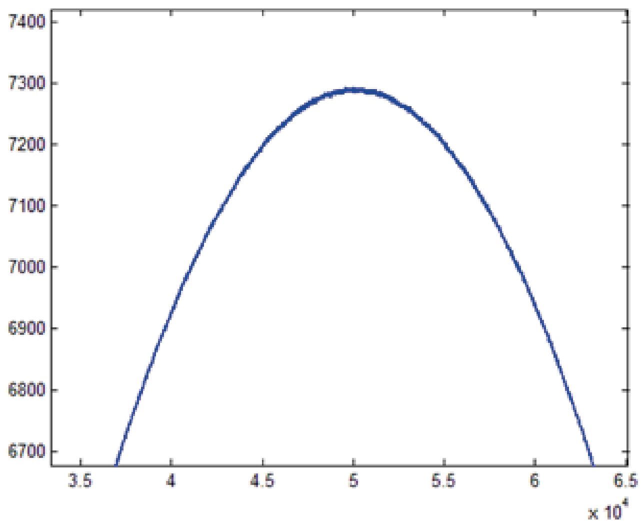


Fig2. After 100 Averaging Cycles

One major advantage of the PCIe/PXIe-9852 Data Average Mode is considerable conservation of memory space. Data averaging using software on the host defines N (number of samples per trace) x R (retrigger events) samples of memory space, while the PCIe/PXIe-9852 Data Average Mode requires only N samples of memory space, since each acquisition is stored in the same onboard buffer before transfer to the PC after averaging. Accordingly, data transfer in Data Average Mode takes far less time, since data size is much smaller.

As well, use of Data Average Mode can significantly reduce CPU loading compared to using software. Since Data Average Mode is FPGA-based, the entire calculation process takes place independent of the CPU. Test data showing comparison of the two solutions is shown, in which the PCIe/PXIe-9852 acquires a 2.0Vpp, 200 kHz continuous sine wave, with 100 retrigger events. Sampling rate of the PCIe/PXIe-9852 is 200 M/s and the amount of data of each acquisition is 100 kS. The test platform utilizes the Intel® Xeon™ CPU E5606 @2.13GHZ. The results show Data Average Mode excelling in performance compared to the software-based solution. As the amount of data and/or retrigger events increase, or in platforms with lower powered processors, the advantages of Data Average Mode actually increase.

	Software	Data Average Mode
Memory space used	100000*100*2 bytes (19 MB)	100000*2 bytes (0.19 MB)
Time taken on acquisition	50 ms	50 ms
Time taken on calculation	215.87 ms	8.306
Data transfer time	15.4 ms	0.154 ms
Total time	281.27 ms	58.46 ms

Table1 Software Based vs. Data Average Mode Signal Averaging

The following block diagrams illustrate the principles as well as comparative benefits of Data Average Mode and software-based solutions.

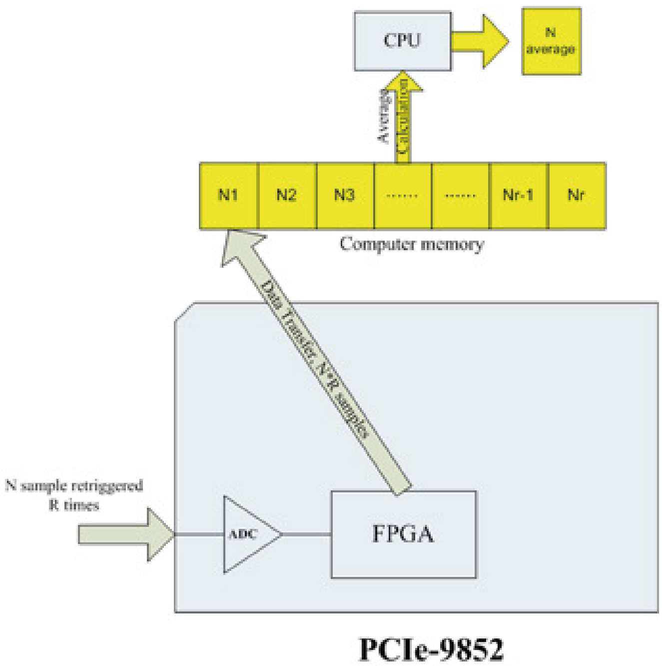


Fig3. Signal Averaging by Software (CPU)

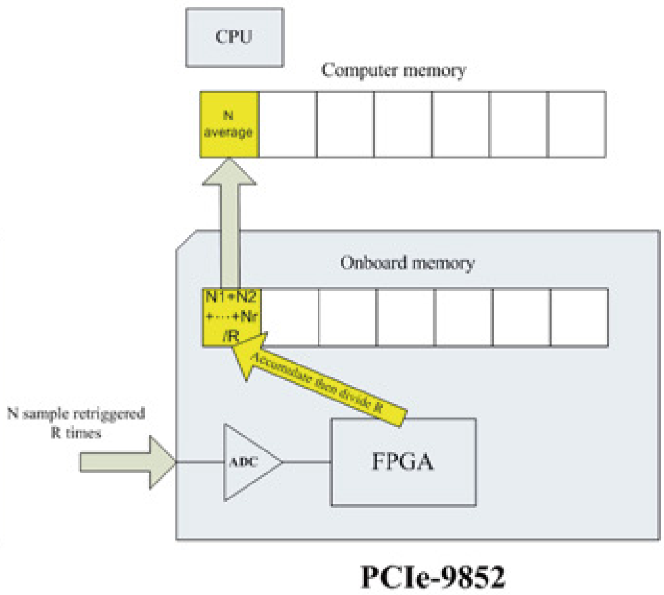
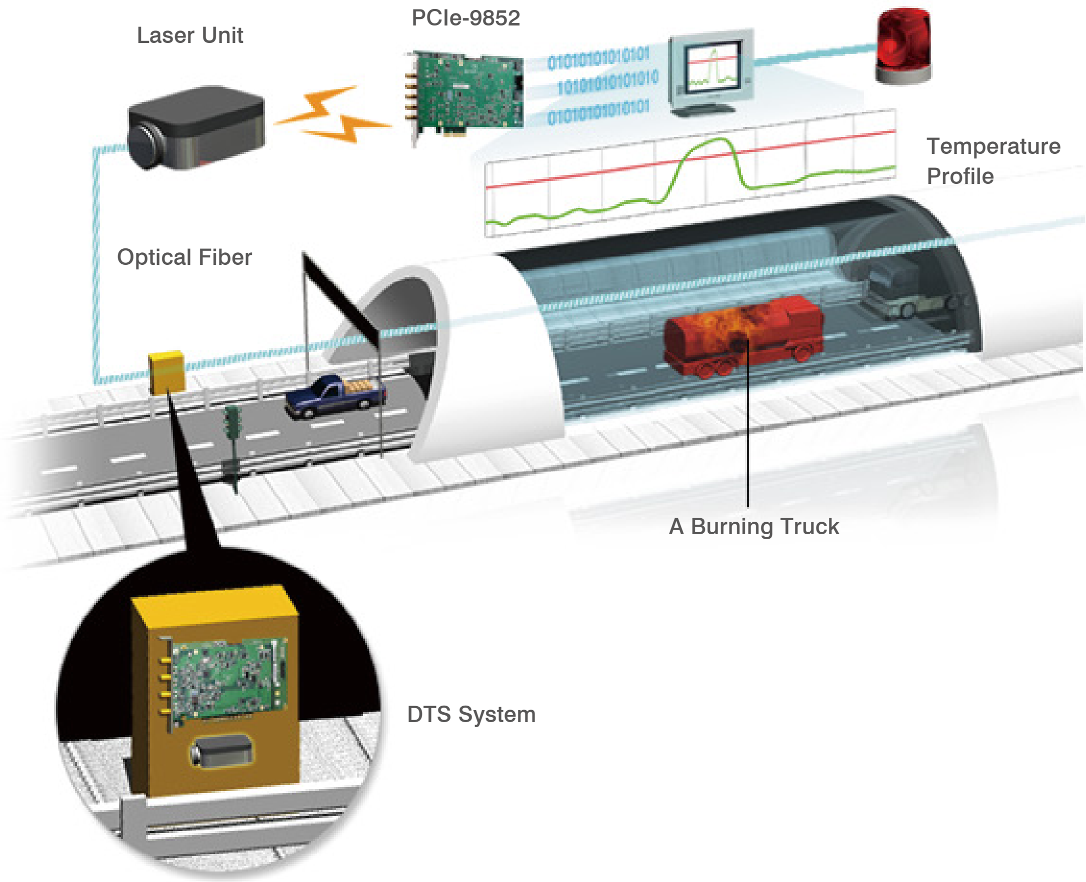


Fig4. Signal Averaging by Data Average Mode

A winning solution for DTS application

Distributed Temperature Sensing (DTS) is a typical application benefiting from signal averaging technology. The DTS, based on Optical Time-Domain Reflectometer (OTDR) instrumentation, measures temperature using optical fiber rather than the conventional thermocouple or thermistor. The process benefits considerably from the cost-effective acquisition of accurate high-resolution temperature measurements in the thousands. DTS can measure temperature profiles along an optical fiber up to 30 km, with pulsed laser coupled to the fiber. Light is backscattered as the pulse propagates through the fiber, with wavelength of the light affected by temperature change in specific positions. Accurate measurement of the difference in signal intensities of the backscattered light generates accurate temperature measurement.

Such high-speed repetitive signals, typically carrying prohibitive levels of unwanted noise, are ideally managed with a high-speed, high-resolution digitizer, with signal averaging of key importance in the application. ADLINK's PCIe-9852 2-CH 200 MS/s 14-Bit high speed digitizer provides exemplary solutions, with the two analog inputs simultaneously receiving both Stokes and anti-Stokes lines generated by the application, and increased high resolution sampling rates easily meeting the requirements of detection distances of 30 km and more. In addition, onboard signal averaging via Data Average Mode isolates even minor detected data from crowded environments.



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ADLINK strives to minimize the total cost of ownership (TCO) of its customers by providing customization and system integration services, maintaining low manufacturing costs, and extending the lifecycle of its products. ADLINK is a global company with headquarters and manufacturing in Taiwan; R&D and integration in Taiwan, China, the US, and Germany; and an extensive network of worldwide sales and support offices.

ADLINK is ISO-9001, ISO-14001, ISO-13485 and TL9000 certified, is an Associate Member of the Intel® Intelligent System Alliance, an Executive Member of PICMG, a Sponsor Member of the PXI Systems Alliance, an Executive Member of PC/104 Consortium, and a Strategic Member of the AXIe Consortium, a member of VMEbus International Trade Association (VITA). ADLINK is a publicly traded company listed on the TAIEX Taiwan Stock Exchange (stock code: 6166).

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