OPENLINE
Bulletin #830

Grayhill INC.

OpenLine® I/O Series 70L & 73L User's Manual

Complete wiring, dimensional, and operational specifications for the I/O modules, I/O mounting racks and accessories can be found in the Grayhill Catalog.

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Other Literature Available:

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1 OPENLINE® MODULE OVERVIEW

The OpenLine® modules are designed to work with Grayhill OpenLine® and OpenDAC™ systems. These modules are primarily dual point modules that minimize space requirements and increase density. Series 70L modules represent all of the digital module types. These modules are discrete, either on or off. The Series 73L modules are analog by nature and measure or control voltage, current, or temperature. Most of the Series 70L modules maintain channel-to-channel isolation as well as field-to-logic isolation while the Series 73L modules only maintain field to logic isolation. The Series 73L analog resolution is primarily 12-bit. The module can handle channel update rates as fast as 500 µsec per channel. For more detailed specifications, refer to specific module drawings.

Note: Throughout this manual, channel 1 and channel 2 are used interchangeably with channel A and B respectively when referring to the two channels of dual point modules.

1.1 Module Communications

OpenLine® modules require three pins to communicate, pin 5 (ground) and pins 7 and 8. For 70L Series modules, pins 7 and 8 are directly tied to the digital input or output of channel 1 and 2, respectively. For the Series 73L modules, pins 7 and 8 are defined as receive and transmit (from the module perspective), respectively.

1.1.1 70L Series Interface

The 70L series digital I/O module interface is a single line per channel. The signal logic is active low. To turn on an output module, the signal line must be pulled to approximately 0 volts. Similarly, when an input module is excited, its logic output is pulled down to approximately 0 volts. The signal lines are internally pulled up to the logic voltage applied to the module allowing the use of open-collector style outputs. Most of the modules operate from 4.5 to 28 Vdc. The maximum current that needs to be sunk by a controlling device is limited to 7ma across the voltage range, which reduces or eliminates additional buffers and drivers.

1.1.2 Series 73L Communications

73L series modules communicate with a controller or master using 2-wire half-duplex asynchronous serial communication at a rate of 115.2 K bits/sec with 0 and 5 volt levels. Commands and data are sent in 8-bit packets with 1 start and 2 stop bits, no parity, and the least significant bit transmitted first. Data should always be sent low byte first. There is no parity, error checking, or error correction done in the communication protocol. Unrecognizable commands will be ignored and discarded.

Modules cannot initiate communications but can only respond to commands received from the controller. Response times to commands range from a few microseconds for the simplest commands to up to 300 milliseconds for the end of a returned message. To insure that multiple byte commands are not misinterpreted, there must be less than 500 microseconds between the start of any one byte and the start of the next byte transmitted. If this time is exceeded, the module will time out and interpret the next byte received as the beginning of a new message and ignore the incomplete command that was previously received.

The module can buffer up to a maximum of 68 bytes (size of largest command with data) before it will lose bytes. To prevent bytes from being missed, send one command at a time and wait for the module to respond completely before sending the next command to the module.

1.2 Series 73L Module Commands

Series 73L module commands are 8-bit in length. For convenience, an ASCII representation of these commands is used. The following command codes are reserved for Grayhill internal use: a, A, c, C, d, D, f, F, g, G, m, M, o, O, r, R, s, S, u, U, x, X, y, Y, z, Z, +, and -.

The protocol for these commands is shown in Table 1. In situations where an upper and lower case letter are used to issue the same command, the upper case letter refers to channel 1 and the lower case letter refers to channel 2.

73L-Ix and 73L-Ox series command protocol: X = Currently Supported, Blank = Not Supported

Command Code Sequence	Direction	Description	I/O Base	73L-Ix	73L-Ox
A	To Module	Read SMP Command	X	X	X
##	To Module	Low Byte of Address			
##	To Module	High Byte of Address			
##	To Module	# of Words to Read (32 max.)			
## (x64)	From Module	Up to 64 Bytes of Data			
a	To Module	Write SMP Command	X	X	X
##	To Module	Low Byte of Address			
##	To Module	High Byte of Address			
##	To Module	# of Words to Write (32 max.)			
## (x64)	To Module	Up to 64 Bytes of Data			
##	From Module	Status – Low Byte (0=Success)			
##	From Module	Status – High Byte (0=Success)			
C, c	To Module	Clear			
C, c	From Module	Acknowledged			
D, d	To Module	Terminate/Disable Execution			
D, d	From Module	Acknowledged			
E, e	To Module	Start/Enable Execution			
E, e	From Module	Acknowledged			
F, f	To Module	Calibrate Full Scale		X	
F, f	From Module	Acknowledged			
G	To Module	Calibrate Gain Setting			X
##	To Module	Gain Byte Channel 1			
##	To Module	Gain Byte Channel 2			
h	To Module	Read Firmware Version		X	X
##	From Module	Firmware Version			
H	To Module	Read Word from EEPROM	X	X	X
##	To Module	# of EEPROM Word			
##	From Module	Low Byte Value			
##	From Module	High Byte Value			

K	To Module	Read Firmware Version		X	X
##	From Module	Status Byte			
m	To Module	A/D Zero		X	
m	From Module	Acknowledged			
M	To Module	A/D Calibrate		X	
M	From Module	Acknowledged			
O	To Module	Calibrate Offset Setting			X
##	To Module	Low Byte Channel 1			
##	To Module	High Byte Channel 1			
##	To Module	Low Byte Channel 2			
##	To Module	High Byte Channel 2			
V	To Module	Read Input Value	X	X	
##	From Module	Low Byte Value Channel 1			
##	From Module	High Byte Value Channel 1			
##	From Module	Low Byte Value Channel 2			
##	From Module	High Byte Value Channel 2			
W	To Module	Write Data Command	X		X
##	To Module	Low Byte Value Channel 1			
##	To Module	High Byte Value Channel 1			
##	To Module	Low Byte Value Channel 2			
##	To Module	High Byte Value Channel 2			
##	From Module	Status Byte			
Y	To Module	Program ID Byte Command		X	X
##	To Module	Channel 1 ID Byte			
##	To Module	Channel 2 ID Byte			
Z, z	To Module	Calibrate Zero Scale		X	
Z, z	From Module	Acknowledged			
+	To Module	Increment Value			X
G, g, O, o, W, w	To Module	Value Type to Increment			
-	To Module	Decrement Value			X
G, g, O, o, W, w	To Module	Value Type to Decrement			

Table 1: Series 73L Command Protocol

1.2.1 Series 73L Normal Operation Commands

Many of the commands listed in Table 1 are not supported by the OpenLine® I/O bases. Typically, under normal operating conditions, only the 'V' command will be used to communicate with Series 73L-I (input) modules and the 'W' command to communicate with Series 73L-O (output) modules. At power up, the base will interrogate all smart modules with the 'H' command to read the module ID located at address 0x00. The SMP read command can also be used for this, but takes longer to execute due to the added bytes needed for the protocol.

1.2.2 SMP Commands

Smart module protocol, or SMP, commands are defined to be the 'A' (SMP read) and 'a' (SMP write) commands. The SMP commands are designed to allow up to 32 words of data to be exchanged with the module at a time. Because communications has the highest priority in the

module, these commands can delay the normal update rate of a module and should be considered to interrupt its normal operation.

1.3 Series 73L Error Conditions

As previously stated, there is no error detection or correction being done for communications with the module. However, a module will monitor internal errors. There are several methods for the module to report these errors depending on whether the module is and input (73L-Ix) or and output (73L-Ox). Any time the module status containing the errors is reported or read, the status bytes are cleared. The module status is volatile so it will be cleared if power is cycled.

1.3.1 Input Module Error Response

Series 73L input modules are typically polled using the 'V' command to read the values for the two channels. Under normal conditions, the module responds with 4 bytes of data (refer to section 1.2), two for channel 1 and two for channel 2. However, the module can preempt this protocol if a critical error has occurred. Critical errors are highlighted within each module type's status word and typically consist of errors such as an invalid EEPROM checksum, EEPROM not responding, A/D converter timeout, open or short circuit detected, or and unknown message received.

The module will set the most significant bit in the 2-byte response for each channel if a critical error has occurred. This bit indicates a critical error for that channel has occurred and the remaining 15 bits should be interpreted as error codes instead of data. Refer to each module type for the definitions of these error codes (see sections 4.3.1, 5.3.1, 6.4, and 7.3.1). Figure 1 and Figure 2 show the format for the data and status bytes that can be returned in response to the 'V' command.

Data: Low Byte							
7	6	5	4	3	2	1	0
Data: Bit 7	Data: Bit 6	Data: Bit 5	Data: Bit 4	Data: Bit 3	Data: Bit 2	Data: Bit 1	Data: Bit 0
Data: High Byte							
7	6	5	4	3	2	1	0
0	0	0	0	Data: Bit 11	Data: Bit 10	Data: Bit 9	Data: Bit 8

Figure 1: Format for Returned Analog Input 12-Bit Data

Status: Low Byte							
7	6	5	4	3	2	1	0
Error: Bit 7	Error: Bit 6	Error: Bit 5	Error: Bit 4	Error: Bit 3	Error: Bit 2	Error: Bit 1	Error: Bit 0
Status: High Byte							
7	6	5	4	3	2	1	0
1	Error: Bit 14	Error: Bit 13	Error: Bit 12	Error: Bit 11	Error: Bit 10	Error: Bit 9	Error: Bit 8

Figure 2: Format for Returned Analog Input Error Code

The error bytes can be returned in place of data for channel 1, channel 2, or both channels, depending on what channels were affected by the critical error. An example data sequence would be:

To Module: 0x56
From Module: 0x31 0x04 0x3C 0x0E

In this example, 0x56 ('V' command) was sent to the module and the module replied that channel 1 was reading 0x0431 and channel 2 was reading 0x0E3C. An example error sequence would be:

To Module: 0x56

From Module: 0x09 0x80 0x3C 0x0E

In this example, 0x56 ('V' command) was sent to the module and the module replied that channel 1 had a critical error and returned the error code 0x8009 (most significant bit is set) while channel 2 was reading a value of 0x0E3C.

1.3.2 Output Module Error Response

Series 73L output modules are typically written to with the value to output on each channel using the 'W' command. In response to receiving this command, the module will return its 1-byte status. Refer to section **7.3.1** for the error code definitions for analog output modules. An example data exchange would be:

To Module: 0x57 0xFF 0x07 0x1C 0x02
From Module: 0x00

In this example, the controller has sent 0x57 ('W' command) to the output module to set channel 1's value to 0x07FF and channel 2's value to 0x021C. The module has responded with no error bits set in its status reply.

1.3.3 Reading Errors with SMP

Another means available to determine what the module errors are is using the Smart Module Protocol (SMP) to read the module status. Both types of modules support this method. The module status is mapped to location 0x0800 within the module memory map. Using the SMP, the status, and consequently any errors, can be read from the module. The SMP command would be:

To Module: 0x41 0x00 0x08 0x01
From Module: 0x00 0x00

In this example, the module has returned a status of 0x0000 showing that no errors have occurred since the last time the status was read or the module powered up.

2 STANDARD PIN-OUT AND WIRING

The OpenLine® modules plug into a base that routes connections out to terminals for the field wiring. There are currently two different form factors for these modules, the standard and doublewide case.

2.1 Standard (Singlewide) Case

The standard case typically contains two discrete I/O channels. Nine .025" square pins are recessed within the bottom of the plastic case. The standard pin definitions are described in Table 2. The standard module case and pin locations are shown in Figure 3. The recommended PCB footprint is shown in Figure 4.

Module Pin #	Series 70L Function	Series 73L Function
1	Channel A+	Channel A+
2	Channel A-	Channel A-
3	Channel B+	Channel B+
4	Channel B-	Channel B-
5	Logic Ground	Logic Ground
6	Vcc (+5VDC)	Vcc (+5VDC)
7	Channel A In/Out	Serial In
8	Channel B In/Out	Serial Out
9	Module ID	Module ID

Table 2: Typical Standard (Singlewide) Pin Definitions

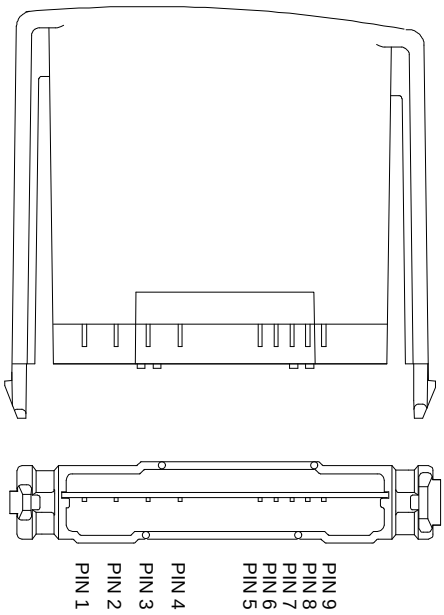

Figure 3: Standard Case and Pin Locations

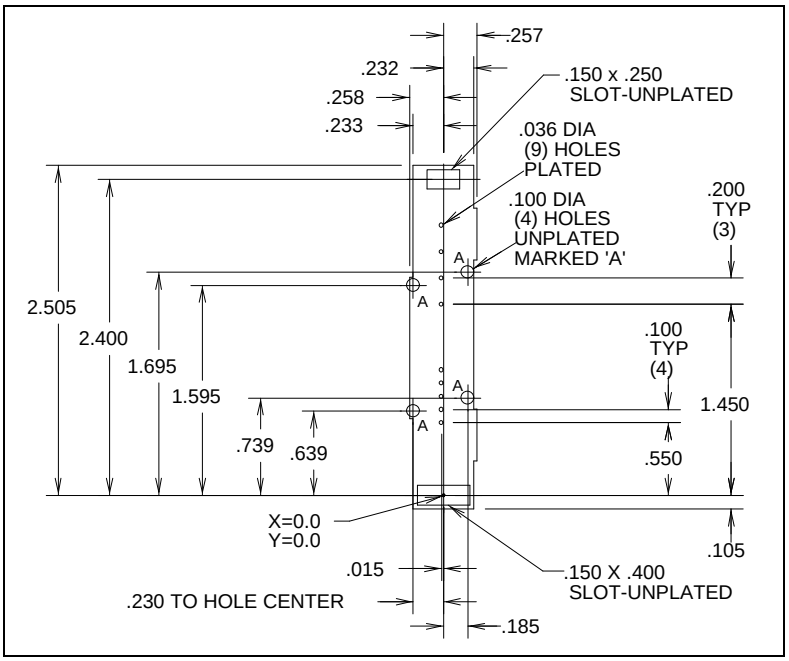

Figure 4: Recommended Standard PCB Footprint

2.2 Doublewide Cases

The doublewide case contains between one and four discrete I/O channels. Eighteen .025" square pins are recessed within the bottom of the plastic case. The doublewide case is designed to fit into two standard case positions that are separated by 0.5". The standard pin definitions are described in Table 3. he doublewide module case and pin locations are shown in Figure 5. The recommended PCB footprint is shown in Figure 6.

Module Pin #	Function	Module Pin #	Function
A1	Channel A1	B1	Channel B1
A2	Channel A2	B2	Channel B2
A3	Channel A3	B3	Channel B3
A4	Channel A4	B4	Channel B4
A5	Logic Ground	B5	Logic Ground
A6	Vcc (+5VDC)	B6	Vcc (+5VDC)
A7	Channel A In/Out	B7	Channel B In/Out
A8	Channel A In/Out	B8	Channel B In/Out
A9	Module ID	B9	Module ID

Table 3: Typical Series 70L Doublewide Pin Definitions

Module Pin #	Function	Module Pin #	Function
A1	Channel A1	B1	Channel B1
A2	Channel A2	B2	Channel B2
A3	Channel A3	B3	Channel B3
A4	Channel A4	B4	Channel B4
A5	Logic Ground	B5	NC
A6	Vcc (+5VDC)	B6	NC
A7	Serial In	B7	NC
A8	Serial Out	B8	NC
A9	Module ID	B9	NC

Table 4: Typical 73L Series Doublewide Pin Definitions

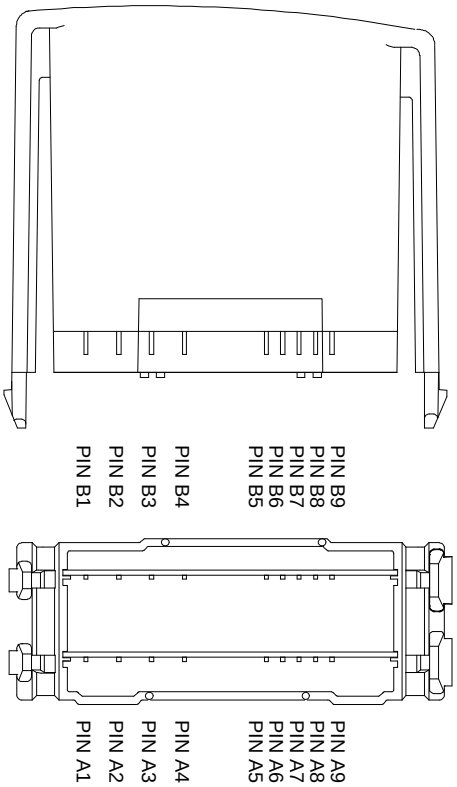

Figure 5: Doublewide Case and Pin Locations

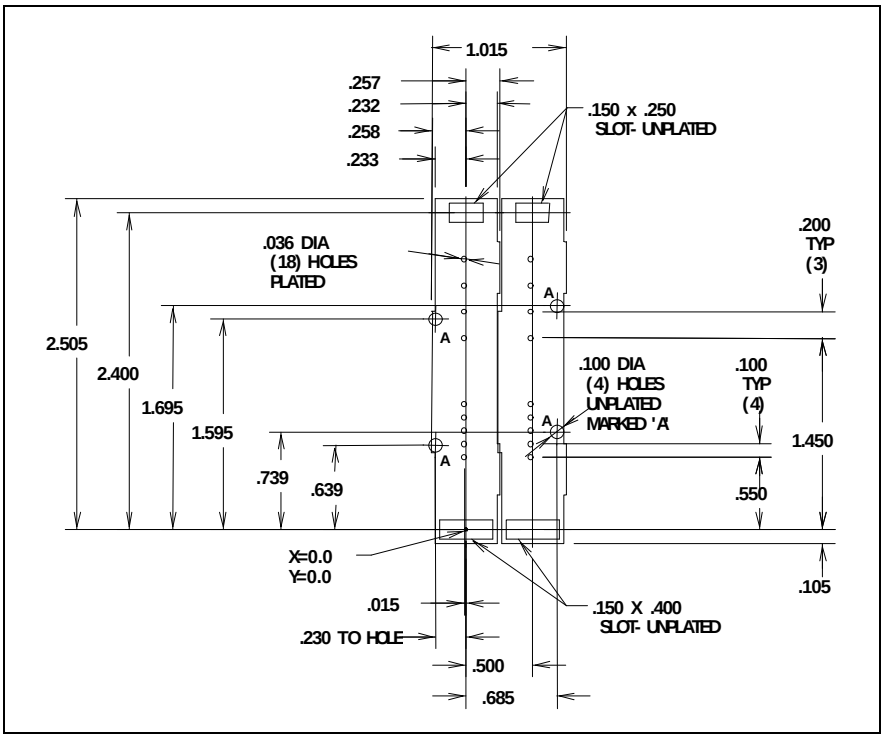

Figure 6: Recommended Doublewide PCB Footprint

2.3 Module ID Pin Values

Each module has a pin that is connected to a precision resistor that can be sensed to determine module type at power up. The 73L series modules are considered smart modules and have more specific ID information stored in memory to further specify what type of module it is (see Table 13). Table 5 shows the resistors defined for the various module categories and the voltage range they produce when tied to a 10 KΩ pull-up resistor.

Module Type	Voltage Range	Module Resistor Value
Digital Input	0V to 0.3V	0 Ω
Digital Output	0.79V to 0.97V	2.15 KΩ 1%
Smart Module	1.44V to 1.92V	5.23 KΩ 1%
No Module	4.70V to 5V	Open Circuit

Table 5: Module ID Pin Resistance Values

2.4 Wiring Diagrams

The OpenLine® modules are designed to plug into an I/O base or rack. Grayhill offers several devices for easy connectivity to these modules. One such I/O base is the 7SLIOB16 8 position (16 channel) dual I/O base. This base is used to provide examples showing how typical wiring might be done to Series 70L and 73L modules. For doublewide wiring, refer to each specific module for the pin definitions and wiring directions.

2.4.1 Digital Module Wiring

The first example given shows channel A of a digital output module wired to a device that will be turned on or off by this channel and is being monitored by a digital input module. The power must be supplied separately since digital output modules do not generate their own power (one exception is the 70L-IDC5S). The voltage of the supply and digital modules used will vary based on the needs of the device being controlled. Refer to Figure 7 for a diagram of how this example can be wired.

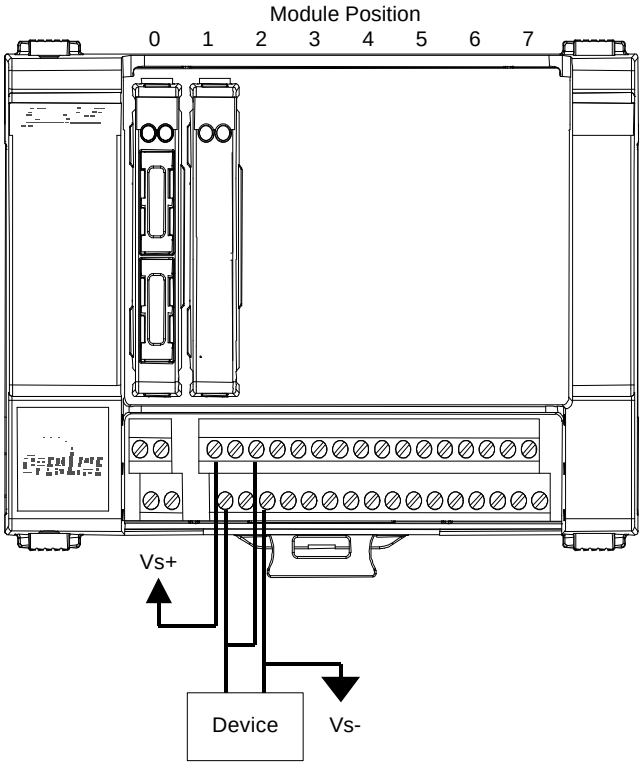

Figure 7: Typical Singlewide Digital Input Wired to a Digital Output

2.4.2 Analog Module Wiring

The next example is an analog output controlling either a voltage-controlled device or a current controlled device. In position 0, channel A of an analog voltage output is wired to a voltage-controlled device and to the input of an analog voltage input located in position 1. In position 6, channel A of an analog current output is wired to a current controlled device and to the input of an analog current input located in position 7. The module types used depend on the voltage or current requirements of the device being controlled or sensed. Refer to Figure 8 for a diagram of how these examples can be wired.

Note: This wiring diagram is given as an example only. It may not always be possible to have an input module wired up with a given device due to loading or other problems that may exceed the parameters of the analog module.

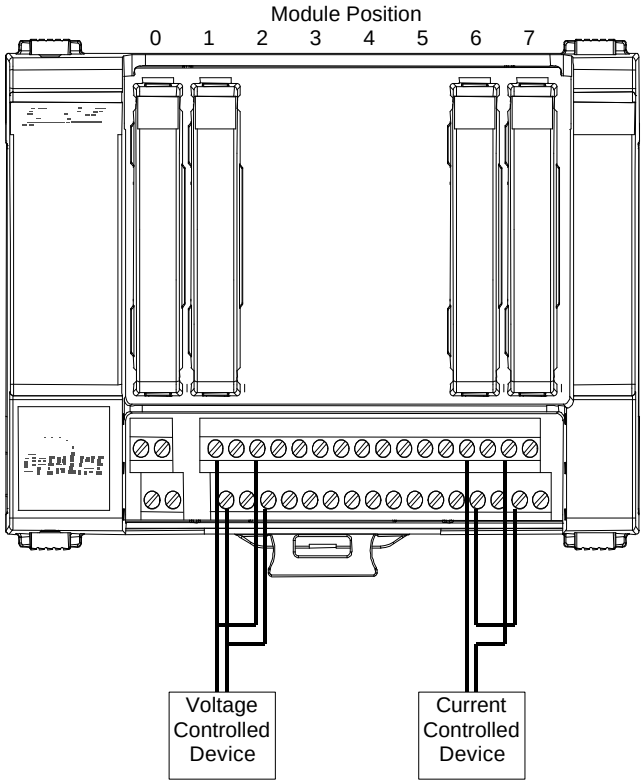

Figure 8: Typical Singlewide Analog Input Wired to an Analog Output

3 SERIES 73L MEMORY MAP

The OpenLine® analog modules all follow the same general memory map. While data descriptions for certain addresses vary between the various types of analog modules, the overall memory map format remains consistent. This format is defined below and data is accessible through the SMP (Smart Module Protocol). All addressing is done on even byte boundaries.

Data Description	Byte Address
EEPROM: Reserved	0x0000 to 0x03FF
EEPROM: User Defined	0x0400 to 0x07FF
RAM	0x0800 to 0x7FFF
Command Area	0x8000 to 0xBFFF
Key Area	0xC000 to 0xCFFF
Undefined	0xD000 to 0xDFFF

Table 6: Series 73L General Memory Map

3.1 EEPROM: Reserved

This section consists of the first 1024 bytes of the SMP address space. The module uses information stored in the first 40 bytes of this area for normal operation. The last word of this 40 byte space is used to checksum the previous 19 words using a simple addition method. Some areas within this section may require an unlock sequence to be successfully executed in order to modify the data.

WARNING: Any data modified in this area may cause the module to operate outside its published parameters.

3.2 EEPROM: User Defined

This area is unused by the module during its operation and is available for the user to define and use as required. Information such as manufacturer, measured units, calibration dates, and other module specific data can be stored in this nonvolatile area.

3.3 RAM

This area of address space is mapped to the module RAM and is volatile. The module uses all data in this area during normal operation.

3.4 Command Area

This area of address space allows special module commands to be executed when written to. The commands are unique to each type of module. Commands are executed immediately upon receipt and will interrupt any other processing being done by the module.

3.5 Key Area

This area of address space is created to allow special keys to be defined to temporarily unlock specific areas of memory. Each key is mapped to a specific address and requires a specific pattern of data to be written to that address. The key will allow the area it protects to be written to only after it is successfully unlocked. It is also volatile so that loss of power will cause the module to lock any previously unlocked areas of memory.

4 OPENLINE® ANALOG INPUTS

The OpenLine® analog input modules share the same memory map and have a part number that follows the format 73L-IIx or 73L-IVx where 'x' represents the specific type of module. The memory map is defined below for the various fields.

Data Description	Byte Address (Hex)	High Byte Definition	Low Byte Definition	Lock Addr.	Lock Key
EEPROM: Reserved					
ID Bytes	0000 to 0001	Channel 2 ID	Channel 1 ID	C002	AAAA
Date Code - Word 1	0002 to 0003	Word 1 high byte	Word 1 low byte	C002	AAAA
Date Code - Word 2	0004 to 0005	Word 2 high byte	Word 2 low byte	C002	AAAA
Channel 1 Zero Factory Default	0006 to 0007	High byte	Low byte	C000	5555
Channel 2 Zero Factory Default	0008 to 0009	High byte	Low byte	C000	5555
Channel 1 Full Factory Default	000A to 000B	High byte	Low byte	C000	5555
Channel 2 Full Factory Default	000C to 000D	High byte	Low byte	C000	5555
Channel 1 Zero Programmed	000E to 000F	High byte	Low byte	C000	5555
Channel 2 Zero Programmed	0010 to 0011	High byte	Low byte	C000	5555
Channel 1 Full Programmed	0012 to 0013	High byte	Low byte	C000	5555
Channel 2 Full Programmed	0014 to 0015	High byte	Low byte	C000	5555
Channel 1 Max Value (Param 1)	0016 to 0017	High byte	Low byte	C000	5555
Channel 2 Max Value (Param 1)	0018 to 0019	High byte	Low byte	C000	5555
Channel 1 Min Value (Param 2)	001A to 001B	High byte	Low byte	C000	5555
Channel 2 Min Value (Param 2)	001C to 001D	High byte	Low byte	C000	5555
Future Use	001E to 0023	High byte	Low byte	C000	5555
Filtering Selection	0024 to 0025	Channel 2	Channel 1	C000	5555
Checksum	0026 to 0027	High byte	Low byte	N/A	N/A
Future Use	0028 to 03FF	High byte	Low byte	-	-
EEPROM: User Defined					
User Defined	0400 to 07FF			-	-
RAM					
Status Word	0800 to 0801	Channel 2	Channel 1	-	-
Future Use	0802 to 7FFF	High byte	Low byte	-	-
Command Area		**Notes**			
Set Channel 1 0 °C Offset	8000 to 8001	Write only. Used for RTDs only			
Set Channel 2 0 °C Offset	8002 to 8003	Write only. Used for RTDs only			
Field Power Reset[1]	8004 to 8005	Write only. Used for 73YY26027 only			
Future Use	8006 to BFFF				
Key Area		**High Byte Definition**	**Low Byte Definition**	**Lock Addr.**	**Lock Key**
Unlock Calibration Data Area	C000 to C001	Write only	Write only	-	5555
Unlock ID and Date Code Area	C002 to C003	Write only	Write only	-	AAAA

Table 7: Analog Input Memory Map

[1] Contact Grayhill for more information.

4.1 EEPROM: Reserved Definitions

This section contains the definitions for all the words specified in this part of the SMP memory map.

4.1.1 ID Bytes

This field contains a unique identification number for each channel that describes the type of module. The ID bytes must be valid numbers in order to be recognized and configured automatically by the OpenLine® system. ID byte definitions are described in section 8 for each type of module. Channel 1's ID is stored in the lower byte while Channel 2's ID is stored in the upper byte.

The ID bytes must be unlocked before being written to. This sequence is implemented using the SMP write command as follows:

0x61 0x02 0xC0 0x01 0xAA 0xAA

0x61 0x00 0x00 0x01 0x## 0x##

In this example 0x61 ('a') is the SMP write command and ## represents the new bytes to be written. The first byte represents the low byte or channel 1's ID and the second byte is the high byte or channel 2's ID. Once the ID field is written to, the area is locked and must be unlocked again for any further modifications.

4.1.2 Date Code

This field contains a 4-byte date code that indicates the time the module was calibrated by Grayhill. The resolution is 2 seconds. When combined with the module ID, this field acts as a unique identifier for each analog module.

The date code bytes must be unlocked before being written to. This sequence is implemented using the SMP write command as follows:

0x61 0x02 0xC0 0x01 0xAA 0xAA

0x61 0x02 0x00 0x02 0x## 0x## 0x## 0x##

In this example 0x61 ('a') is the SMP write command and ## represents the new bytes to be written. The date code byte definition is described in section 9.

4.1.3 Factory Defaults

This field contains the factory defaults for the zero and full-scale calibration data for both channel 1 and 2. Under normal circumstances, this data (from 0x0006 to 0x000D) will exactly match the programmed calibration values (address 0x000E to 0x0015). The factory default values are not used by the module during its operation, but are stored to allow the module to be returned to its original settings should the programmed calibration values be changed.

The factory default bytes must be unlocked before being written to. This sequence is implemented using the SMP write command as follows:

0x61 0x00 0xC0 0x01 0x55 0x55

0x61 0x06 0x00 0x04 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x##

In this example 0x61 (‘a’) is the SMP write command and ## represents the new bytes to be written.

4.1.4 Programmed Calibration Values

This field contains the programmed calibration values used by the module to scale the input range. The zero scale value is the data point where the minimum range is sensed and the full scale value is the data point where the maximum range is sensed. These fields can be modified to contain any value between 0 and 0x1FFF to change the range of the specific module.

For example, channel 1 zero scale value is 0x1F3E but it is determined that the module is always a few counts low, returning 0x0000 before the actual minimum range is reached. The zero scale value can be changed to 0x1F3F (or higher if needed) to increase the window slightly and allow the module to return values for readings that were previously below the minimum range. The module will automatically rescale its 12-bit output so that 0 will correspond to this slightly lower value.

WARNING: Changing the programmed calibration values may alter the accuracy and other published parameters of the module.

The programmed calibration bytes must be unlocked before being written to. This sequence is implemented using the SMP write command as follows:

0x61 0x00 0xC0 0x01 0x55 0x55

0x61 0x0E 0x00 0x04 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x##

In this example 0x61 (‘a’) is the SMP write command and ## represents the new bytes to be written.

4.1.5 Max. and Min. Values

This field contains locations to store a one-word value to represent the minimum and maximum values for each channel. These values are not used by the module but reflect the ranges for each channel. For example, if a 0-5V input is being used to measure the input from a dial controlling the speed of a motor, the maximum value might be changed from 0x0005 to 0x03E8 to represent 1000 rpm (0x03E8) instead of 5 volts (0x0005).

4.1.6 Future Use

These fields are not currently defined but are reserved for future use.

4.1.7 Filtering Selection

This field is used to enable and select the various software filters designed into the module. The bytes are defined as shown in Figure 9.

Filtering Selection: Low Byte							
7	6	5	4	3	2	1	0
X	X	X	X	X	Ch1 Filter Enable	Ch1 Filter Type	Ch1 Filter Depth
Filtering Selection: High Byte							
7	6	5	4	3	2	1	0
X	X	X	X	X	Ch2 Filter Enable	Ch2 Filter Type	Ch2 Filter Depth

Figure 9: Filtering Selection Bit Definitions

4.1.7.1 Ch1/Ch2 Filter Enable

When set, this bit will enable the software filter for the respective channel. When cleared, this bit disables all software filtering for the respective channel. If filtering is enabled, the module update rate of new data will be slowed due to the increased amount of processing required. However, since filtering is enabled, the stop response of the module is also slowed according to the graphs in section 10.

4.1.7.2 Ch1/Ch2 Filter Type

When set, this bit selects a moving average filter for the respective channel. When cleared, this bit selects an exponential averaging filter for the respective channel. The step responses for the various filtering selections are shown in section 10.

4.1.7.3 Ch1/Ch2 Filter Depth

When set, this bit selects 16 samples to be used for the moving average or a 0.125 weighting factor for the exponential average for the respective channel. When cleared, this bit selects 8 samples to be used for the moving average or a 0.25 weighting factor for the exponential average for the respective channel. The step responses for the various filtering depths are shown in section 10.

4.1.8 Checksum

This field is read only and is used to provide a means to verify the integrity of the first 19 words in the reserved area of the EEPROM. The checksum is calculated by summing, without a carry, all the even (lower) bytes and all the odd (upper) bytes. The resulting two bytes are stored in the lower and upper bytes, respectively, of the checksum.

4.2 EEPROM: User Defined

This section of the EEPROM is available for the end user to store data local to the module. Contact Grayhill for information on having data stored in this section of memory at the factory to meet specific requirements.

4.3 RAM

This section contains the definitions for all the words specified in this part of the SMP memory map.

4.3.1 Status Word

These two bytes contain the module status and are read only. Reading these two bytes will cause any error flags set in the status to be cleared. Under some circumstances, the status word is sent back instead of data when a critical error has occurred (see section 1.3.1). This will also cause all status bits to be cleared. When the status is returned instead of data, it is distinguished from the data by having the most significant bit set. The status word is defined in Figure 10.

Status Word: Low Byte							
7	6	5	4	3	2	1	0
Invalid EE Checksum	EE Not Responding	A/D Timeout	0	0	Ch1 Old Data	Ch1 Under Range	Ch1 Over Range
Status Word: High Byte							
7	6	5	4	3	2	1	0
Event Indicator	Low Voltage/ Reset	Unknown Message	0	0	Ch2 Old Data	Ch2 Under Range	Ch2 Over Range

Note: Shaded bit descriptions are critical errors that, when set, force the status word to be returned in place of data.

Figure 10: Analog Input Status Word Bit Definitions

4.3.1.1 Invalid EE Checksum

This bit is set whenever the checksum stored in the EEPROM does not match the checksum calculated. The checksum is verified anytime data is written to the first 20 words of EEPROM. If this bit is set, the last command that wrote to the checksummed area of the EEPROM should be repeated. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

4.3.1.2 EE Not Responding

This bit is set if the EEPROM does not respond when data is being either read or written to the device. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

4.3.1.3 A/D Timeout

This bit is set if the A/D converter fails to convert within a predetermined amount of time. If set, the most recent data returned may be old. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

4.3.1.4 Ch1/Ch2 Old Data

This bit is set for the respective channel if the module is queried for data before it has updated the data since the last request.

4.3.1.5 Ch1/Ch2 Under Range

This bit is set for the respective channel if that channel detects the input went below the minimum calibrated value for the channel.

4.3.1.6 Ch1/Ch2 Over Range

This bit is set for the respective channel if that channel detects the input exceeded the maximum calibrated value for the channel.

4.3.1.7 Event Indicator

The event indicator is set any time any other bit in the status word is set. It is used to distinguish status information from actual data (bit position will be zero for actual data). The event indicator and all other bits in the status word are cleared whenever the status is reported or read.

4.3.1.8 Low Voltage/Reset

This bit is set whenever the module powers up or experiences a reset due to a low voltage condition.

4.3.1.9 Unknown Message

This bit is set whenever a message is received that does not follow the specific protocol for the module. Causes for this bit being set can range from too much time between bytes in a multiple byte message to simply trying to write to a protected area of memory before unlocking it. This bit is used to convey that the module did not act on the message that was sent. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

4.3.2 Future Use

These fields are not currently defined but are reserved for future use.

4.4 Command Area

Refer to section 6.5 for more detail.

4.5 Key Area

This area of the memory map is write only and is used to unlock other areas for one-time writes. This adds a measure of security to ensure that critical areas are not overwritten accidentally. Each key is assigned an address and a data value that, when sent properly, will unlock the protected area for one write only.

4.5.1 Unlock Calibration Data Area

This key protects the calibration data area located from 0x0006 to 0x0025. This area contains the factory defaults, the current calibration as well as other checksummed values used by the module. This key should be used whenever one or more words in the calibration data area is to be modified. The command sequence would use the SMP write command as follows:

0x61 0x00 0xC0 0x01 0x55 0x55

4.5.2 Unlock ID and Date Code Area

This key protects the module IDs and date code located from 0x0000 to 0x0005. This key should be used whenever one or more words in this area is to be modified. The command sequence would use the SMP write command as follows:

0x61 0x02 0xC0 0x01 0xAA 0xAA

4.6 Normal Operation

During normal operation, the analog input responds to commands sent to it. Typically the 'V' command is sent to poll the module for the values on its input channels. Most modules are designed to update new data every millisecond for two separate channels (refer to the individual module data sheets for actual specifications). However, some module settings may affect this update capability such as the software filtering selections (refer to section 4.1.7). Also, some commands may interrupt the normal processing of the module such as the SMP ('A' and 'a') commands (refer to section 1.2.2). When this occurs, the "old data" flag in the status word might be set if the module has not had sufficient time to update the data since the last report.

5 OPENLINE® ANALOG THERMOCOUPLES

The OpenLine® analog thermocouple modules share the same memory map and have a part number that follows the format 73L-ITCx where 'x' represents the specific type of module. The memory map is defined below for the various fields.

Data Description	Byte Address (Hex)	High Byte Definition	Low Byte Definition	Lock Addr.	Lock Key
EEPROM: Reserved					
ID Bytes	0000 to 0001	Channel 2 ID	Channel 1 ID	C002	AAAA
Date Code - Word 1	0002 to 0003	Word 1 high byte	Word 1 low byte	C002	AAAA
Date Code - Word 2	0004 to 0005	Word 2 high byte	Word 2 low byte	C002	AAAA
Channel 1 Zero Factory Default	0006 to 0007	High byte	Low byte	C000	5555
Channel 2 Zero Factory Default	0008 to 0009	High byte	Low byte	C000	5555
Channel 1 Full Factory Default	000A to 000B	High byte	Low byte	C000	5555
Channel 2 Full Factory Default	000C to 000D	High byte	Low byte	C000	5555
Channel 1 Zero Programmed	000E to 000F	High byte	Low byte	C000	5555
Channel 2 Zero Programmed	0010 to 0011	High byte	Low byte	C000	5555
Channel 1 Full Programmed	0012 to 0013	High byte	Low byte	C000	5555
Channel 2 Full Programmed	0014 to 0015	High byte	Low byte	C000	5555
Channel 1 Max Value (Param 1)	0016 to 0017	High byte	Low byte	C000	5555
Channel 2 Max Value (Param 1)	0018 to 0019	High byte	Low byte	C000	5555
Channel 1 Min Value (Param 2)	001A to 001B	High byte	Low byte	C000	5555
Channel 2 Min Value (Param 2)	001C to 001D	High byte	Low byte	C000	5555
OWD Threshold	001E to 001F	Channel 2	Channel 1	C000	5555
Future Use	0020 to 0023	High byte	Low byte	C000	5555
Filtering Selection	0024 to 0025	Channel 2	Channel 1	C000	5555
Checksum	0026 to 0027	High byte	Low byte	N/A	N/A
Future Use	0028 to 03FF	High byte	Low byte	-	-
EEPROM: User Defined					
User Defined	0400 to 07FF			-	-
RAM					
Status Word	0800 to 0801	Channel 2	Channel 1	-	-
Future Use	0802 to 7FFF	High byte	Low byte	-	-
Command Area		**Notes**			
Set Channel 1 0 °C Offset	8000 to 8001	Write only. Used for RTDs only			
Set Channel 2 0 °C Offset	8002 to 8003	Write only. Used for RTDs only			
Field Power Reset	8004 to 8005	Write only. Used for 73YY26027 only			
Future Use	8004 to BFFF				
Key Area		**High Byte Definition**	**Low Byte Definition**	**Lock Addr.**	**Lock Key**
Unlock Calibration Data Area	C000 to C001	Write only	Write only	-	5555
Unlock ID and Date Code Area	C002 to C003	Write only	Write only	-	AAAA

Table 8: Analog Thermocouple Memory Map

5.1 EEPROM: Reserved Definitions

Refer to section 4.1 for more detail.

5.1.1 OWD Threshold

This field will determine the number of counts that must jump from one reading to the next reading in order to more quickly detect an open wire on the circuit. The maximum jump that can be specified in this field is 255 or 0x00FF. The default setting for this field is 16 counts or 0x0010. A value of 0 in this field will disable the algorithm from detecting open wire conditions. When disabled, open wires will cause the returned temperature to appear to drift up until exceeding the maximum temperature for the module and finally crossing a threshold for open wires, causing the error condition to be reported. When enabled, any time the temperature changes more than the specified amount in one cycle (approximately 2.5 mS), an open wire error will be reported. However, even under the most drastic changes, thermocouples change very slowly and rarely exceed the default value.

5.2 EEPROM: User Defined

This section of the EEPROM is available for the end user to store data local to the module. Contact Grayhill for information on having data stored in this section of memory at the factory to meet specific requirements.

5.3 RAM

This section contains the definitions for all the words specified in this part of the SMP memory map.

5.3.1 Status Word

These two bytes contain the module status and are read only. Reading these two bytes will cause any error flags set in the status to be cleared. Under some circumstances, the status word is sent back instead of data when a critical error has occurred (see section 1.3.1). This will also cause all status bits to be cleared. When the status is returned instead of data, it is distinguished from the data by having the most significant bit set. The status word is defined in Figure 11.

Status Word: Low Byte							
7	6	5	4	3	2	1	0
Invalid EE Checksum	EE Not Responding	A/D Timeout	0	Ch1 Open Circuit	Ch1 Old Data	Ch1 Under Range	Ch1 Over Range
Status Word: High Byte							
7	6	5	4	3	2	1	0
Event Indicator	Low Voltage/ Reset	Unknown Message	0	Ch2 Open Circuit	Ch2 Old Data	Ch2 Under Range	Ch2 Over Range

Note: Shaded bit descriptions are critical errors that, when set, force the status word to be returned in place of data.

Figure 11: Analog Thermocouple Status Word Bit Definitions

5.3.1.1 Invalid EE Checksum

This bit is set whenever the checksum stored in the EEPROM does not match the checksum calculated. The checksum is verified anytime data is written to the first 20 words of EEPROM. If this bit is set, the last command that wrote to the checksummed area of the EEPROM should be repeated. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

5.3.1.2 EE Not Responding

This bit is set if the EEPROM does not respond when data is being either read or written to the device. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

5.3.2 A/D Timeout

This bit is set if the A/D converter fails to convert within a predetermined amount of time. If set, the most recent data returned may be old. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

5.3.2.1 Ch1/Ch2 Open Circuit

This bit is set for the respective channel if the channel detects that an open circuit has occurred on the wires. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

5.3.2.2 Ch1/Ch2 Old Data

This bit is set for the respective channel if the module is queried for data before it has updated the data since the last request.

5.3.2.3 Ch1/Ch2 Under Range

This bit is set for the respective channel if that channel detects the input went below the minimum calibrated value for the channel.

5.3.2.4 Ch1/Ch2 Over Range

This bit is set for the respective channel if that channel detects the input exceeded the maximum calibrated value for the channel.

5.3.2.5 Event Indicator

The event indicator is set any time any other bit in the status word is set. It is used to distinguish status information from actual data (bit position will be zero for actual data). The event indicator and all other bits in the status word are cleared whenever the status is reported or read.

5.3.2.6 Low Voltage / Reset

This bit is set whenever the module powers up or experiences a reset due to a low voltage condition.

5.3.2.7 Unknown Message

This bit is set whenever a message is received that does not follow the specific protocol for the module. Causes for this bit being set can range from too much time between bytes in a multiple byte message to simply trying to write to a protected area of memory before unlocking it. This bit is used to convey that the module did not act on the message that was sent. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

5.3.3 Future Use

These fields are not currently defined but are reserved for future use.

5.4 Command Area

Refer to section 6.5 for more detail.

5.5 Key Area

Refer to section 4.5 for more detail.

5.6 Normal Operation

The analog thermocouples perform similarly to the analog input modules. Refer to section 4.6 for more information.

6 OPENLINE® ANALOG RTDS

The OpenLine® analog RTD modules share the same memory map and have a part number that follows the format 73L-ITRx where 'x' represents the specific type of module. The memory map is defined below for the various fields.

Data Description	Byte Address (Hex)	High Byte Definition	Low Byte Definition	Lock Addr.	Lock Key
EEPROM: Reserved					
ID Bytes	0000 to 0001	Channel 2 ID	Channel 1 ID	C002	AAAA
Date Code - Word 1	0002 to 0003	Word 1 high byte	Word 1 low byte	C002	AAAA
Date Code - Word 2	0004 to 0005	Word 2 high byte	Word 2 low byte	C002	AAAA
Channel 1 Zero Factory Default	0006 to 0007	High byte	Low byte	C000	5555
Channel 2 Zero Factory Default	0008 to 0009	High byte	Low byte	C000	5555
Channel 1 Full Factory Default	000A to 000B	High byte	Low byte	C000	5555
Channel 2 Full Factory Default	000C to 000D	High byte	Low byte	C000	5555
Channel 1 Zero Programmed	000E to 000F	High byte	Low byte	C000	5555
Channel 2 Zero Programmed	0010 to 0011	High byte	Low byte	C000	5555
Channel 1 Full Programmed	0012 to 0013	High byte	Low byte	C000	5555
Channel 2 Full Programmed	0014 to 0015	High byte	Low byte	C000	5555
Channel 1 Max Value (Param 1)	0016 to 0017	High byte	Low byte	C000	5555
Channel 2 Max Value (Param 1)	0018 to 0019	High byte	Low byte	C000	5555
Channel 1 Min Value (Param 2)	001A to 001B	High byte	Low byte	C000	5555
Channel 2 Min Value (Param 2)	001C to 001D	High byte	Low byte	C000	5555
Channel 1 0 °C Offset	001E to 001F	High byte	Low byte	C000	5555
Channel 2 0 °C Offset	0020 to 0021	High byte	Low byte	C000	5555
OWD Threshold	0022 to 0023	High byte	Low byte	C000	5555
Filtering Selection	0024 to 0025	Channel 2	Channel 1	C000	5555
Checksum	0026 to 0027	High byte	Low byte	N/A	N/A
Future Use	0028 to 03FF	High byte	Low byte	-	-
EEPROM: User Defined					
User Defined	0400 to 07FF			-	-
RAM					
Status Word	0800 to 0801	Channel 2	Channel 1	-	-
Future Use	0802 to 7FFF	High byte	Low byte	-	-
Command Area		**Notes**			
Set Channel 1 0 °C Offset	8000 to 8001	Write only. Used for RTDs only			
Set Channel 2 0 °C Offset	8002 to 8003	Write only. Used for RTDs only			
Field Power Reset	8004 to 8005	Write only. Used for 73YY26027 only			
Future Use	8004 to BFFF				
Key Area		**High Byte Definition**	**Low Byte Definition**	**Lock Addr.**	**Lock Key**
Unlock Calibration Data Area	C000 to C001	Write only	Write only	-	5555
Unlock ID and Date Code Area	C002 to C003	Write only	Write only	-	AAAA

Table 9: Analog RTD Memory Map

6.1 EEPROM: Reserved Definitions

This section contains the definitions for all the words specified in this part of the SMP memory map.

6.1.1 ID Bytes

Refer to section 4.1.1 for more detail.

6.1.2 Date Code

Refer to section 4.1.2 for more detail.

6.1.3 Factory Defaults

Refer to section 4.1.3 for more detail.

6.1.4 Programmed Calibration Values

Refer to section 4.1.4 for more detail.

6.1.5 Max. and Min. Values

Refer to section 4.1.5 for more detail.

6.1.6 Ch1/Ch2 0 °C Offset Values

These fields store an offset that is added or subtracted from the value read from each respective channel. This value is only used by the 73L-ITR100 module. The offset is applied to the read value inside the module before it is linearized which eliminates errors resulting from the linearization process. Refer to section 6.5 for more information concerning these fields.

6.1.7 OWD Threshold

This field will determine the number of counts that must jump from one reading to the next reading in order to more quickly detect a wire fault on the circuit. The maximum jump that can be specified in this field is 255 or 0x00FF. The default setting for this field is 16 counts or 0x0010. A value of 0 in this field will disable the algorithm from detecting wire fault conditions. When disabled, wire faults may cause the returned temperature to appear to drift up or down until exceeding the maximum or minimum temperature for the module. It then crosses a threshold for wire faults, causing the error condition to be reported. When enabled, any time the temperature changes more than the specified amount in one cycle (approximately 2.5 msec), a wire fault error will be reported

6.1.8 Filtering Selection

Refer to section 4.1.7 for more detail.

6.1.9 Checksum

Refer to section 4.1.8 for more detail.

6.2 EEPROM: User Defined

This section of the EEPROM is available for the end user to store data local to the module. Contact Grayhill for information on having data stored in this section of memory at the factory to meet specific requirements.

6.3 RAM

This section contains the definitions for all the words specified in this part of the SMP memory map.

6.4 Status Word

These two bytes contain the module status and is read only. Reading these two bytes will cause any error flags set in the status to be cleared. Under some circumstances, the status word is sent back instead of data when a critical error has occurred (see section 1.3.1). This will also cause all status bits to be cleared. When the status is returned instead of data, it is distinguished from the data by having the most significant bit set. The status word is defined in Figure 12.

Status Word: Low Byte							
7	6	5	4	3	2	1	0
Invalid EE Checksum	EE Not Responding	A/D Timeout		Ch1 Wire Fault	Ch1 Old Data	Ch1 Under Range	Ch1 Over Range
Status Word: High Byte							
7	6	5	4	3	2	1	0
Event Indicator	Low Voltage / Reset	Unknown Message		Ch2 Wire Fault	Ch2 Old Data	Ch2 Under Range	Ch2 Over Range

Note: Shaded bit descriptions are critical errors that, when set, force the status word to be returned in place of data.

Figure 12: Analog RTD Status Word Bit Definitions

6.4.1.1 Invalid EE Checksum

This bit is set whenever the checksum stored in the EEPROM does not match the checksum calculated. The checksum is verified anytime data is written to the first 20 words of EEPROM. If this bit is set, the last command that wrote to the checksummed area of the EEPROM should be repeated. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

6.4.1.2 EE Not Responding

This bit is set if the EEPROM does not respond when data is being either read or written to the device. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

6.4.1.3 A/D Timeout

This bit is set if the A/D converter fails to convert within a predetermined amount of time. If set, the most recent data returned may be old. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

6.4.1.4 Ch1/Ch2 Wire Fault

This bit is set for the respective channel if the channel detects that an open or short circuit has occurred on the wires. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

6.4.1.5 Ch1/Ch2 Old Data

This bit is set for the respective channel if the module is queried for data before it has updated the data since the last request.

6.4.1.6 Ch1/Ch2 Under Range

This bit is set for the respective channel if that channel detects the input went below the minimum calibrated value for the channel.

6.4.1.7 Ch1/Ch2 Over Range

This bit is set for the respective channel if that channel detects the input exceeded the maximum calibrated value for the channel.

6.4.1.8 Event Indicator

The event indicator is set any time any other bit in the status word is set. It is used to distinguish status information from actual data (bit position will be zero for actual data). The event indicator and all other bits in the status word are cleared whenever the status is reported or read.

6.4.1.9 Low Voltage / Reset

This bit is set whenever the module powers up or experiences a reset due to a low voltage condition.

6.4.1.10 Unknown Message

This bit is set whenever a message is received that does not follow the specific protocol for the module. Causes for this bit being set can range from too much time between bytes in a multiple byte message to simply trying to write to a protected area of memory before unlocking it. This bit is used to convey that the module did not act on the message that was sent. When set, this bit will force the status word to be returned in place of data (see section 1.3.1).

6.4.2 Future Use

These fields are not currently defined but are reserved for future use.

6.5 Command Area

This area of the SMP address space is write-only and is used to initiate special commands for the 73L series modules. These commands are executed immediately after being received and parsed unless otherwise specified.

6.5.1 Set Channel 1 0° Offset

When this command is executed, the 73L-ITR100 will read the current resistance on channel 1 and subtract that from the ideal value of a 100Ω RTD at 0 °C (which is 100Ω). The result is stored as the 0 °C offset. This command is useful in zeroing out any lead resistance or error there might be in the RTD connections.

To properly execute this command, the RTD element connected to channel 1 should be held at precisely 0 °C with the length of wire being used for its installation connected up with it. This temperature can be approximated with an ice bath. However, the melting point of ice can vary depending on pressure and impurities in the water. Also, keep in mind that because of the size of many RTDs, the device may not be at completely the same temperature or may take several minutes for the RTD element to thoroughly adjust to the temperature. Once the input to channel 1 is at 0 °C, the command should be executed using the SMP write command as follows:

0x61 0x00 0x80 0x00

No data needs to be written to cause the command to be executed. The module will respond with an acknowledgement of 0x00 if the command was executed. If the value is still slightly off, the process can be repeated, or the offset value can be read from the EEPROM and then rewritten with a slightly different value to affect the change needed.

6.5.2 Set Channel 2 0° Offset

When this command is executed, the 73L-ITR100 will read the current resistance on channel 2 and subtract that from the ideal value of a 100Ω RTD at 0 °C (which happens to be 100Ω). The

result is stored as the 0°C offset. This command is useful in zeroing out any lead resistance or error there might be in the RTD connections.

To properly execute this command, the RTD element connected to channel 2 should be held at precisely 0°C with the length of wire being used for its installation connected up with it (refer to section 6.5.1 for more information on this). Once the input to channel 2 is at 0 °C, the command should be executed using the SMP write command as follows:

0x61 0x02 0x80 0x00

No data needs to be written to cause the command to be executed. The module will respond with an acknowledgement of 0x00 if the command was executed. If the value is still slightly off, the process can be repeated, or the offset value can be read from the EEPROM and then rewritten with a slightly different value to affect the change needed.

6.6 Key Area

Refer to section 4.5 for more detail.

6.7 Normal Operation

The analog RTD modules perform similarly to the analog input modules. Refer to section 4.6 for more information.

7 OPENLINE® ANALOG OUTPUTS

The OpenLine® analog output modules share the same memory map and have a part number that follows the format 73L-OIx or 73L-OVx where 'x' represents the specific type of module. The memory map is defined below for the various fields.

Data Description	Byte Address (Hex)	High Byte Definition	Low Byte Definition	Lock Addr.	Lock Key
EEPROM: Reserved					
ID Bytes	0000 to 0001	Channel 2 ID	Channel 1 ID	C002	AAAA
Date Code - Word 1	0002 to 0003	Word 1 high byte	Word 1 low byte	C002	AAAA
Date Code - Word 2	0004 to 0005	Word 2 high byte	Word 2 low byte	C002	AAAA
Unipolar Gain Factory Default	0006 to 0007	Channel 2	Channel 1	C000	5555
Ch1 Unipolar Offset Factory Default	0008 to 0009	High byte	Low byte	C000	5555
Ch2 Unipolar Offset Factory Default	000A to 000B	High byte	Low byte	C000	5555
Bipolar Gain Factory Default	000C to 000D	Channel 2	Channel 1	C000	5555
Ch1 Bipolar Offset Factory Default	000E to 000F	High byte	Low byte	C000	5555
Ch2 Bipolar Offset Factory Default	0010 to 0011	High byte	Low byte	C000	5555
Unipolar Gain	0012 to 0013	Channel 2	Channel 1	C000	5555
Channel 1 Unipolar Offset	0014 to 0015	High byte	Low byte	C000	5555
Channel 2 Unipolar Offset	0016 to 0017	High byte	Low byte	C000	5555
Bipolar Gain	0018 to 0019	Channel 2	Channel 1	C000	5555
Channel 1 Bipolar Offset	001A to 001B	High byte	Low byte	C000	5555
Channel 2 Bipolar Offset	001C to 001D	High byte	Low byte	C000	5555
Channel 1 Default Output	001E to 001F	High byte	Low byte	C000	5555
Channel 2 Default Output	0020 to 0021	High byte	Low byte	C000	5555
Power Supply Selection[2]	0022 to 0023	High byte	Low byte	C000	5555
Future Use	0024 to 0025	High byte	Low byte	C000	5555
Checksum	0026 to 0027	High byte	Low byte	N/A	N/A
Future Use	0028 to 03FF	High byte	Low byte	-	-
EEPROM: User Defined					
User Defined	0400 to 07FF			-	-
RAM					
Status Word	0800 to 0801	0000	Channel 1 & 2	-	-
Future Use	0802 to 7FFF	High byte	Low byte	-	-
Command Area		**Notes**			
Future Use	8000 to BFFF				
Key Area		**High Byte Definition**	**Low Byte Definition**	**Lock Addr.**	**Lock Key**
Unlock Calibration Data Area	C000 to C001	Write only	Write only	-	5555
Unlock ID and Date Code Area	C002 to C003	Write only	Write only	-	AAAA

Table 10: Analog Output Memory Map

7.1 EEPROM: Reserved Definitions

This section contains the definitions for all the words specified in this part of the SMP memory map.

[2] Power Supply Selection is used only for 73YY26028. Contact Grayhill for more information. All other outputs reserve this for future use.

7.1.1 ID Bytes
Refer to section 4.1.1 for more detail.

7.1.2 Date Code
Refer to section 4.1.2 for more detail.

7.1.3 Factory Defaults
This field contains the factory defaults for the zero and full-scale calibration data for both channel 1 and 2. Under normal circumstances, this data (from 0006 to 0011) will exactly match the programmed calibration values (address 0012 to 001D). The factory default values are not used by the module during its operation, but are stored to allow the module to be returned to its original settings should the programmed calibration values be changed.

The factory default bytes must be unlocked before being written to. This sequence is implemented using the SMP write command as follows:

0x61 0x00 0xC0 0x01 0x55 0x55

0x61 0x06 0x00 0x06 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x##

In this example 0x61 (‘a’) is the SMP write command and ## represents the new bytes to be written.

7.1.4 Programmed Calibration Values
This field contains the programmed calibration values used by the module to scale the input range. The zero scale value is the data point where the minimum range is sensed and the full scale value is the data point where the maximum range is sensed. These fields can be modified to contain any value between 0x00 and 0xFF for gain, or 0x0000 and 0x0FFF for offset to change the calibration of the specific module.

For example, channel 1 offset value is 0x131 but it is determined that the module is always a few bits low, outputting a slightly negative voltage when it should be absolute zero. The offset value can be changed to 0x12F (or lower if needed) to increase the voltage slightly. To increase the offset of the output module, decrease the value stored for the offset. To increase the gain of the output module, increase the value stored for the gain. It is important to remember that changing the offset or the gain will affect both the low end and high-end readings of the module. Therefore, changing one value will require the other value to be verified to ensure that it is still accurate.

WARNING: Changing the programmed calibration values will alter the accuracy and other published parameters of the module.

The programmed calibration bytes must be unlocked before being written to. This sequence is implemented using the SMP write command as follows:

0x61 0x00 0xC0 0x01 0x55 0x55

0x61 0x12 0x00 0x06 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x## 0x##

In this example 0x61 ('a') is the SMP write command and ## represents the new bytes to be written.

7.1.5 Ch1/Ch2 Default Output

This field is used to enable and select the various software filters designed into the module. The bytes are defined as shown in Figure 13.

Channel 1 Default Output: Low Byte							
7	6	5	4	3	2	1	0
Ch1 Def. Value Bit 7	Ch1 Def. Value Bit 6	Ch1 Def. Value Bit 5	Ch1 Def. Value Bit 4	Ch1 Def. Value Bit 3	Ch1 Def. Value Bit 2	Ch1 Def. Value Bit 1	Ch1 Def. Value Bit 0
Channel 1 Default Output: High Byte							
7	6	5	4	3	2	1	0
Ch1 W.D. Enable	W.D T.O. Period Bit 2	W.D T.O. Period Bit 1	W.D T.O. Period Bit 0	Ch1 Def. Value Bit 11	Ch1 Def. Value Bit 10	Ch1 Def. Value Bit 9	Ch1 Def. Value Bit 8
Channel 2 Default Output: Low Byte							
7	6	5	4	3	2	1	0
Ch2 Def. Value Bit 7	Ch2 Def. Value Bit 6	Ch2 Def. Value Bit 5	Ch2 Def. Value Bit 4	Ch2 Def. Value Bit 3	Ch2 Def. Value Bit 2	Ch2 Def. Value Bit 1	Ch2 Def. Value Bit 0
Channel 2 Default Output: High Byte							
7	6	5	4	3	2	1	0
Ch2 W.D. Enable	X	X	X	Ch2 Def. Value Bit 11	Ch2 Def. Value Bit 10	Ch2 Def. Value Bit 9	Ch2 Def. Value Bit 8

Figure 13: Ch1/Ch2 Default Output Bit Definitions

7.1.5.1 Ch1/Ch2 Default Value

This is the default value that the respective channel will go to should the communications watchdog time out and the watchdog is enabled for that channel. The value can be anything between 0x000 and 0xFFF (0 and 4095).

7.1.5.2 Ch1/Ch2 WD Enable

When set, this bit enables the default value (refer to section 7.1.5.1) for the respective channel to be output should the communication watchdog time out. If cleared, this bit disables the communication watchdog for that channel and will cause the module to hold the last value received until a new write command is successfully received.

If the communication watchdog is enabled at power-up, the output will initialize to the minimum output value. The module will not enable the watchdog until the first write command is received. This is due to the fact that various systems may take different amounts of time to power up and establish communications. However, once the first write command is received, the watchdog will operate normally. The watchdog can be enabled or disabled at any time for either channel.

7.1.5.3 W.D.T.O. Period

This field sets the watchdog timeout period. The 3-bit field determines the amount of time allowed between the beginning of any two valid messages to the module. Both channels use this field to determine this duration. The timeout periods are described in Table 11.

Watchdog Timeout Period Bit 2	Watchdog Timeout Period Bit 1	Watchdog Timeout Period Bit 0	Min. Timeout Period (milliseconds)
0	0	0	68 mS
0	0	1	140 mS
0	1	0	212 mS
0	1	1	288 mS
1	0	0	356 mS
1	0	1	426 mS
1	1	0	496 mS
1	1	1	568 mS

Table 11: Communication Watchdog Timeout Period

7.1.6 Future Use

These fields are not currently defined but are reserved for future use.

7.1.7 Checksum

This field is read only and is used to provide a means to verify the integrity of the reserved area of the EEPROM. The checksum is calculated by summing, without a carry, all the even (lower) bytes and all the odd (upper) bytes. The resulting two bytes are stored in the lower and upper bytes, respectively, of the checksum.

7.2 EEPROM: User Defined

This section of the EEPROM is available for the end user to store data local to the module. Contact Grayhill for information on having data stored in this section of memory at the factory to meet specific requirements.

7.3 RAM

This section contains the definitions for all the words specified in this part of the SMP memory map.

7.3.1 Status Word

This byte contains the module status. Reading these two bytes will cause any error flags set in the status to be cleared. The status low byte of the status word is returned after any successful 'W' command. The status word is defined in Figure 14.

Status Word: Low Byte							
7	6	5	4	3	2	1	0
Event Indicator	Invalid Checksum	EE Write Protect	Unknown Message	Comm. WD Timeout	0	Ch2 Open Circuit	Ch1 Open Circuit
Status Word: High Byte							
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Figure 14: Analog Output Status Word Bit Definitions

7.3.1.1 Event Indicator

The event indicator is set any time any other bit in the status word is set. The event indicator and all other bits in the status word are cleared whenever the status is reported or read.

7.3.1.2 Invalid Checksum

This bit is set whenever the checksum stored in the EEPROM does not match the checksum calculated. The checksum is verified anytime data is written to the first 20 words of EEPROM. If this bit is set, the last command that wrote to the checksummed area of the EEPROM should be repeated. When set, this bit will force the status word to be returned in place of data.

7.3.1.3 EE Write Protect

This bit is set if there was an attempt to write to a protected part of the EEPROM memory.

7.3.1.4 Unknown Message

This bit is set whenever a message is received that does not follow the specific protocol for the module. Causes for this bit being set can range from too much time between bytes in a multiple byte message to simply trying to write to a protected area of memory before unlocking it. This bit is used to convey that the module did not act on the message that was sent. When set, this bit will force the status word to be returned in place of data.

7.3.1.5 Comm. WD Timeout

This bit is set whenever either channel has enabled the communication watchdog and the timeout period was exceeded by any two valid consecutive messages.

7.3.1.6 Ch1/Ch2 Open Circuit

These bits are only updated for modules that have open circuit detection capability like the 73YY26028 0-24 mA output. These bits indicate that an open circuit was detected on the respective channel.

The open circuit detection is only enabled when two successive writes with a value greater than or equal to 0x064 are sent to the output channel. The open circuit detection is disabled immediately upon receipt of a write command with a value less than 0x064.

7.3.2 Future Use

These fields are not currently defined but are reserved for future use.

7.4 Command Area

Reserved for future use.

7.5 Key Area

This area of the memory map is write only and is used to unlock other areas for one-time writes. This adds a measure of security to ensure that critical areas are not overwritten accidentally. Each key is assigned an address and a data value that, when sent properly, will unlock the protected area for one write only.

7.5.1 Unlock Calibration Data Area

Refer to section 4.5.1 for more information.

7.5.2 Unlock ID and Date Code Area

Refer to section 4.5.2 for more information.

7.6 Normal Operation

During normal operation, the analog output module responds to commands sent to it. Typically the 'W' command is sent to write the values to its output channels. Most modules are designed to update new data every millisecond for two separate channels (refer to the individual module data sheets for actual specifications). While the data is updated immediately (before the status response is sent), the actual output reading may take several microseconds to settle. Also, some commands may interrupt the normal processing of the module such as the SMP ('A' and 'a') commands (refer to section 1.2.2).

When writing data to each of the 12-bit output channels, it is important to right justify the 12 bits within the 16-bit field. For example, the command to set channel 1 to full scale and channel 2 to half scale would be:

0x57 0xFF 0x0F 0x00 0x08

In this example 0x57 ('W' command) is sent with the data for channel 1 and channel 2 of 0x0FFF and 0x0800 respectively. The most significant four bits must remain zero. If any of these bits are set, the module will interpret this as a value in excess of its range and simply set the output to 0x0FFF (full scale). For example, if 0x1000 were written to channel 1, the full-scale value of 0x0FFF would be written to the output for this channel.

8 MODULE ID DEFINITIONS

Each Series 73L module has a programmed ID for each channel. This is stored in the first word of EEPROM memory (refer to section 4.1.1 for more information). Each module ID is a code between 0x00 and 0xFF (0 and 255).

8.1 Module Classifications

The upper 4 bits of the module ID are used to place the module into a classification. The bit definitions for the module ID are as shown in Figure 15.

Status Word: High Byte							
7	6	5	4	3	2	1	0
Output / Input	Class Bit 2	Class Bit 1	Class Bit 0	Module ID Bit 3	Module ID Bit 2	Module ID Bit 1	Module ID Bit 0

Figure 15: Module ID Bit Definitions

8.1.1 Output / Input

When set, this bit indicates the module is an output. When clear, the module is an input.

8.1.2 Class Bit[2:0]

These bits represent the module classification. This classification is determined as shown in Table 12.

Device Type	Class Bit 2	Class Bit 1	Class Bit 0
Digital / No Module	0	0	0
Analog Voltage	0	0	1
Analog Current	0	1	0
Analog Temperature	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Table 12: Module Classification Bit Definitions

Note: Device ID 0x00 indicates no module present.

8.2 Module ID Definitions

The 73L series module ID's are defined in Table 13.

Part Number	Type Description	ID	Notes
Voltage Inputs			
73L-IV50M	0 to 50 mV	0x10	
73L-IV100M	0 to 100 mV	0x11	
73L-IV1	0 to 1 V	0x12	
73L-IV5	0 to 5 V	0x13	
73L-IV10	0 to 10 V	0x14	
73L-IV5B	-5 to +5 V	0x15	
73L-IV10B	-10 to +10 V	0x16	
Current Inputs			
73L-II420	4 to 20 mA	0x20	
73L-II020	0 to 20 mA	0x21	
73YY26026	0 to 21 mA	0x22	25.5V supply, 240 Vrms protection, 1000V isolation
Temperature Inputs			
73L-ITCJ	J Thermocouple	0x30	-210 to 1200 °C
73L-ITCK	K Thermocouple	0x31	-100 to 1372 °C
73L-ITCT	T Thermocouple	0x32	-240 to 400 °C
73L-ITCR	R Thermocouple	0x33	0 to 1767 °C
73L-ITR100	100 Ω PT	0x38	2-wire RTD, -50 to 350 °C
73L-ITR1000	1000 Ω PT	0x39	2-wire RTD, -50 to 350 °C
73L-ITR10	10 Ω PT	0x3A	2-wire RTD, -50 to 350 °C
73YY26022	100 Ω PT	0x3B	2-wire RTD, 0 to 100 °C
73L-ITR4100	100 Ω PT	0x3C	4-wire RTD, -50 to 350 °C
73YY26029-1	25 to 190 Ω Res.	0x3D	4-wire resistance
73YY26025	25 to 190 Ω Res.	0x3E	3-wire resistance, doublewide, 240 Vrms protection
73L-ITR3100	100 Ω PT	0x3F	3-wire RTD, -50 to 350 °C
Voltage Outputs			
73L-OV5	0 to 5 V	0x90	
	-2.5 to 2.5 V	0x91	
73L-OV10	0 to 10 V	0x92	
73L-OV5B	-5 to +5 V	0x93	
73L-OV10B	-10 to +10 V	0x94	
Current Outputs			
73L-OI020	0 to 20 mA	0xA0	
73L-OI420	4 to 20 mA	0xA1	
73L-OI024	0 to 24 mA	0xA2	
73YY26028	0 to 21 mA	0xA3	1000V Isolation, open wire detection, 240 Vrms protection
Smart			
		0x40	Reserved
		0xC0	Reserved
		0xC1	Reserved

		0xC2	Reserved
Digital Inputs			
70L-I Series	Standard Digital	0x01	Input
70YY27012	24VAC/DC	0x02	Open wire detection
70YY27013	Contact Closure	0x03	Open wire detection
70YY27014	80-140VAC/DC	0x04	Open wire detection
70YY27015	10-32 VDC / 15-32 VAC	0x05	
70YY27016	90-140 VAC/DC	0x06	
70YY27017	180-280 VAC/DC	0x07	
Digital Outputs			
70L-O Series	Standard Digital	0x80	
70YY29002	Form C EM Relay	0x81	3A@250VAC/3A@48VDC w/ blown fuse & open wire detection. Aromat DSP1 relays. Doublewide case. 4.0A fast blow fuse.
70YY29004	Form C EM Relay	0x82	1A@220VAC/0.625A@250VDC with blown fuse & open wire detection. Siemens V23042 relays. Doublewide case. 1.0A fast blow fuse.
70YY29006	Form C EM Relay	0x83	2A@48VAC/2A@48VDC (1K cycles) with blown fuse & open wire detection. Siemens V23042 relays. Doublewide case. 4.0A fast blow fuse.
70YY29008	Form C EM Relay	0x84	2A@115VAC/1A@115VDC with blown fuse & open wire detection. Siemens V23042 relays. Doublewide case. 2.0A fast blow fuse.
70YY27018	200 VDC, 1A	0x85	1A@200VDC dual solid state output.
70YY27019	60 VDC, 2A	0x86	2A@60VDC dual solid state output.
70YY27020	280 VAC, 2A	0x87	2A@280VAC dual solid state output.
Miscellaneous			
	No Module Present	0x00	

Table 13: Module ID Definitions

Note: Shaded module ID's are reserved by Grayhill.

9 MODULE DATE CODE DEFINITION

Each module uses a 2-byte date code that is written into the EEPROM as the final step in the module calibration process. This date code has a resolution down to 2 seconds and, when used in conjunction with the module ID field, provides a unique identifier for each module. The date code rolls over every one hundred years. The data code bit definitions are described in Figure 16.

Date Code Word 1: Low Byte							
7	6	5	4	3	2	1	0
Min. Bit 2	Min. Bit 1	Min. Bit 0	Sec. Bit 4	Sec. Bit 3	Sec. Bit 2	Sec. Bit 1	Sec. Bit 0
Date Code Word 1: High Byte							
7	6	5	4	3	2	1	0
Hour Bit 4	Hour Bit 3	Hour Bit 2	Hour Bit 1	Hour Bit 0	Min. Bit 5	Min. Bit 4	Min. Bit 3
Date Code Word 2: Low Byte							
7	6	5	4	3	2	1	0
Week Bit 4	Week Bit 3	Week Bit 2	Week Bit 1	Week Bit 0	Day Bit 2	Day Bit 1	Day Bit 0
Date Code Word 2: High Byte							
7	6	5	4	3	2	1	0
Year Bit 6	Year Bit 5	Year Bit 4	Year Bit 3	Year Bit 2	Year Bit 1	Year Bit 0	Week Bit 5

Figure 16: Date Code Bit Definitions

The ranges and resolutions for the various fields are described in Table 14.

Field	Range	Resolution
Seconds	0 to 29	2 seconds
Minutes	0 to 59	1 minute
Hour	0 to 23	1 hour
Day	0 to 6	Sunday = 0, Saturday = 6
Week	1 to 52	1 week
Year	0 to 99	1 year

Table 14: Date Code Ranges and Resolutions

10 MODULE FILTERING SELECTIONS

Most Series 73L-I modules allow a software filter to be selected in addition to the filtering that is already done to the analog signal. The step response for the various filters is shown in the following figures. These software filters do not represent the actual step response of the module. The actual module response must factor in both the analog filtering and software filtering for the complete module characteristic response. The sample number is relative to the module (occurring once every millisecond) and not to the polling of the module which may vary.

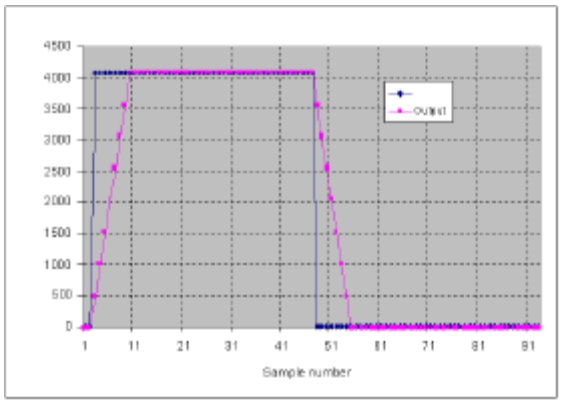

Figure 17: Moving Average with Depth of 8.

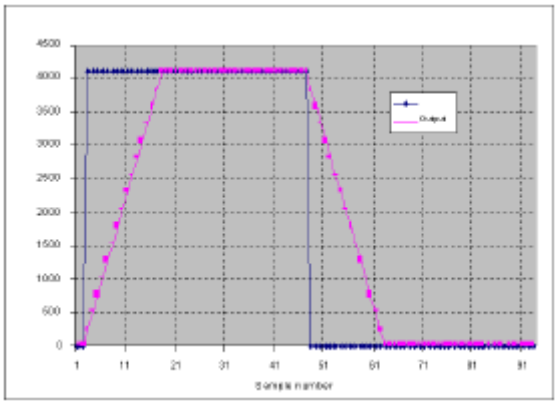

Figure 18: Moving average with Depth of 16.

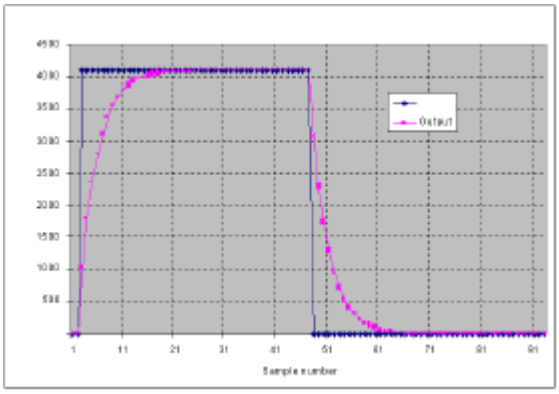

Figure 19: Exponential Average with Weight of 1/4.

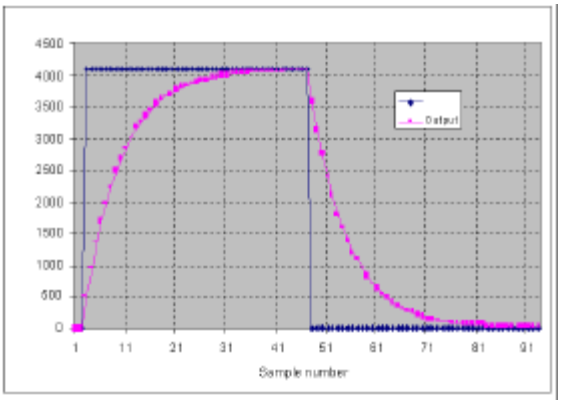

Figure 20: Exponential Average with Weight of 1/8.