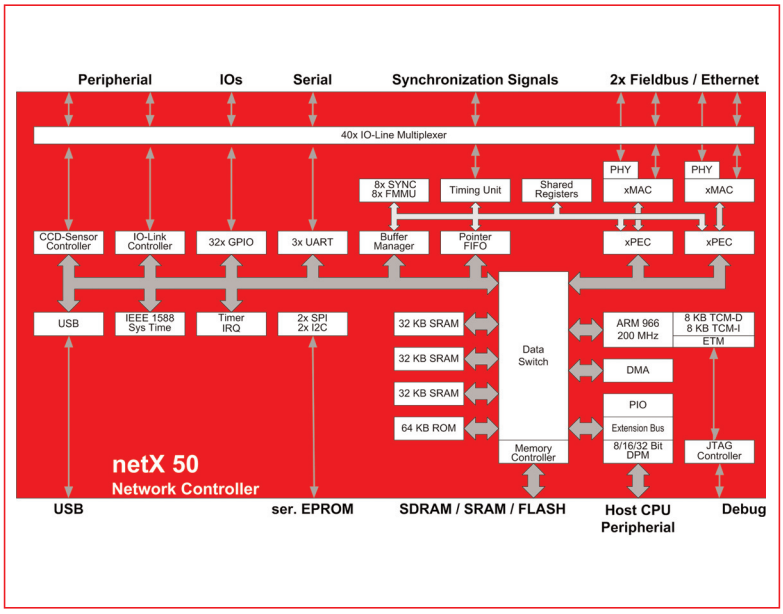
netX 50 – networX on chip
The future of communication

Description

- Flexible “high end” network controller with host interface or single chip solution for digital I/Os
- Two communication channels as Real-Time Ethernet with PHY or fieldbus
- New system architecture optimized for communication and high data throughput
- 32-Bit / 200 MHz CPU ARM 966 with 112 KB SRAM / 64 KB ROM and extensive periphery
- Dual-Port-Memory, Extension bus or digital I/Os
- IO-Link Controller, 8 channels
- CCD-Sensor Controller



The netX is a highly integrated network controller with a new system architecture optimized for communication and maximum data throughput.

Via an integrated dual-port memory it works as an companion chip to a host CPU and realises the complete scope of industrial communication from fieldbus systems up to the Real-Time Ethernet systems. Allows the application no own CPU the host interface can be configured as Extension Bus or directly as digital input and output.
The 32-Bit CPU ARM 966E-S is clocked with 200 MHz and has 112 KB internal RAM and 64 KByte ROM memory. The memory can be expanded flexible by the 32-Bit memory controller with SDRAM, SRAM or FLASH externally.
Extensive periphery functions, serial interfaces such as UART, USB, SPI, I²C, as well as the integrated IO-Link and CCD controller allows a large scope of applications.
The central data switch and the free configurable communication channels with its own intelligence are the unique selling proposition of the netX as an “high end” network controller.

The data switch connects via five data paths to the ARM CPU and the communication, Host and DMA controllers with the memory or the peripheral units. In this way the controllers transmit their data in parallel, contrary to the traditional sequential architecture with only one common data bus and additional bus allocation cycles.

The controllers of the two communication channels are structured on two levels and are identical to each other. They consist of dedicated ALUs and special logic units that receive their protocol functions via Microcode. For Ethernet the PHYs are integrated which means that the external circuit for Ethernet is reduced to passive componets: transformer and RC components.
The Medium-Access-Controller xMAC sends or receives the data according to the respective bus access process and encrypts or converts these into Byte depictions.
The Protocol Execution Controller xPEC compiles these into data packets and controls the telegram traffic. Large data amoutns are exchanged in DMA blocks over the memory of the ARM. In addition, every channel has a Dual-port-memory available for status information. Alternatively a triple buffer logic is implemented for a conflict free data exchange which always gives the address of the next free buffer.

With the intelligent communication ALUs, the netX carries out the most varied protocols and protocol combinations on one chip – an absolutely new feature in industrial communication technology.

netX
networX on chip
Hilscher
NETX 50 A
0711IU600 ARM

Supported Real-Time Ethernet systems

EtherCAT Technology Group
EtherNet/IP
ETHERNET POWERLINK
PROFINET INDUSTRIAL ETHERNET
SERCOS interface
Modbus IDA MEMBER

Supported Fieldbus systems

Master only
ASI INTERFACE
CANopen
Slave only
CC-Link
DeviceNet
PROFIBUS PROCESS FIELD BUS

netX 50 – details

Technical Data

Core			
Processor	ARM 966E-S, 200 MIPS, ARMv5TE-command set with DSP-extension		
Tightly coupled memory	8 KByte Data, 8 KByte Instruction		
Internal Memory			
RAM	96 KByte		
ROM	64 KByte with Bootloader		
Ethernet-Interface			
Ports	2 x 10BASE-T / 100BASE-TX, Half- / Full-Duplex, IEEE 1588 time stamp		
PHY	Integrated, Auto-Negotiation, Auto-Crossover		
Real-Time-Ethernet	EtherCAT with eight FMMUs and eight Sync-Manager		
	Ethernet/IP		
	Modbus IDA		
	Powerlink with integrated Hub		
	PROFINET RT and IRT with integrated Switch		
	SERCOS-III		
Fieldbus-Interface	If Ethernet is not used, the communication channels are available as Fieldbus-Interfaces.		
	The systems can be combined as desired.		
Fieldbus	AS-Interface, Master only		
	CANopen, Master and Slave		
	CC-Link, Slave only		
	DeviceNet, Master and Slave		
	PROFIBUS, Master and Slave		
Periphery			
IO-Link Controller	8 Channels, automatically direction control		
CCD-Sensor Controller	max. 50 MHz, 640x480 Pixel, free configurable data format		
IEEE 1588 System Time	32-Bit second counter, 32-Bit Nano second counter		
USB	Revision 1.1, 12 MBaud Full-Speed, Host- or Device-Mode		
UART	16550 compatible, max. 3 MBaud, RTS/CTS support	Quantity	3
I²C			
SPI	Master- and Slave-Mode, max. 10 MHz, 3 Chip-Select-Signals		
General I/Os	3.3 V / 6 mA	Quantity	32
Status LEDs	2 LEDs two-colors, 3.3 V / 9 mA		
Memory-Interface			
Memory bus	32-Bit-Databus / 24-Bit-Address bus		
Address region	256 MByte SDRAM / 64 MByte Flash		
Memory modules	SDRAM, SRAM, Flash		
Host-Interface			
Dual-port-memory-mode	8 / 16 / 32-Bit-Databus, 64 KByte configurable in 8 Blocks, emulated by internal RAM		
Extension-Mode	8/16-Bit-Databus, 24-Bit-Address bus, Bustiming adjustable		
PIO-Mode	Freely programmable Inputs and Outputs	Quantity	53
Debug-Interface			
JTAG	ARM-Processor and Boundary-Scan		
ETM	Embedded Trace Macrocell, ETM9 V2 Medium Size		
Operating conditons / housings / various data			
System cycles	200 MHz ARM / 100 MHz Periphery		
Signal level		V	3.3
Power supply	for Core	V	1.5
	for Input/Output	V	3.3
Operating temperature	without heat sink	°C	–40..+70
	with heat sink 10°/W	°C	–40..+85
Storage temperature		°C	–65..+150
Power consumption	PHYs switched off	W	0.8
	PHYs switched on	W	1.2
Housing	PBGA, 1 mm raster	Pins	324
	Dimensions	mm	19 x 19

Note: *All technical data can be altered without notice.*

Product Overview

Article designation	*Article number*	*Article*
netX 50	2230.000	netX 50

Note

For application Hilscher master protocol a master license must be ordered separately. These will delivered as Security EPROMs and is provided in the design. Further information: www.hilscher.com/netx

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