16Z001_SMB – I2C SMBus Controller IP Core

- **FPGA IP Core**
- **SMBus master interface**
- **Wishbone slave interface**

The SMBus controller is a bridge between an SMBus and a Wishbone interface. The SMBus features master capabilities, while the Wishbone interface features slave capability.
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SMBus is a two-wire, bidirectional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.
The bridge can be a master on the SMBus, providing quick send byte, receive byte, write byte, write word, read byte, read word, block read, block write commands.
The SMBus controller conforms to the ALI M1543C PCI-ISA bus bridge with Super I/O & Fast IR SMBus interface. Revisions 7 and later feature multi-master capability (latest software drivers required!).
The Wishbone interface core is compliant to the Wishbone Rev B.3 Wishbone Classic interface.
MEN IP cores are described in standard VHDL language and the standard Wishbone bus is used as the system interface.
By using IP cores, application-specific functions can be performed flexibly and individually in the FPGA on a growing range of MEN CPU boards. These IP cores can be assembled from the MEN function library and reconfigured, combined with IP cores from other providers or even completely redeveloped as required. The FPGA behaves just like a standard PCI component. The FPGA functions are loaded by software when the system is booted and are available in less than 1 s. On PowerPC® platforms the FPGA can be dynamically updated during operation. On Pentium® platforms FPGA updates are also possible in the boot Flash during operation and are then available once the system is rebooted.

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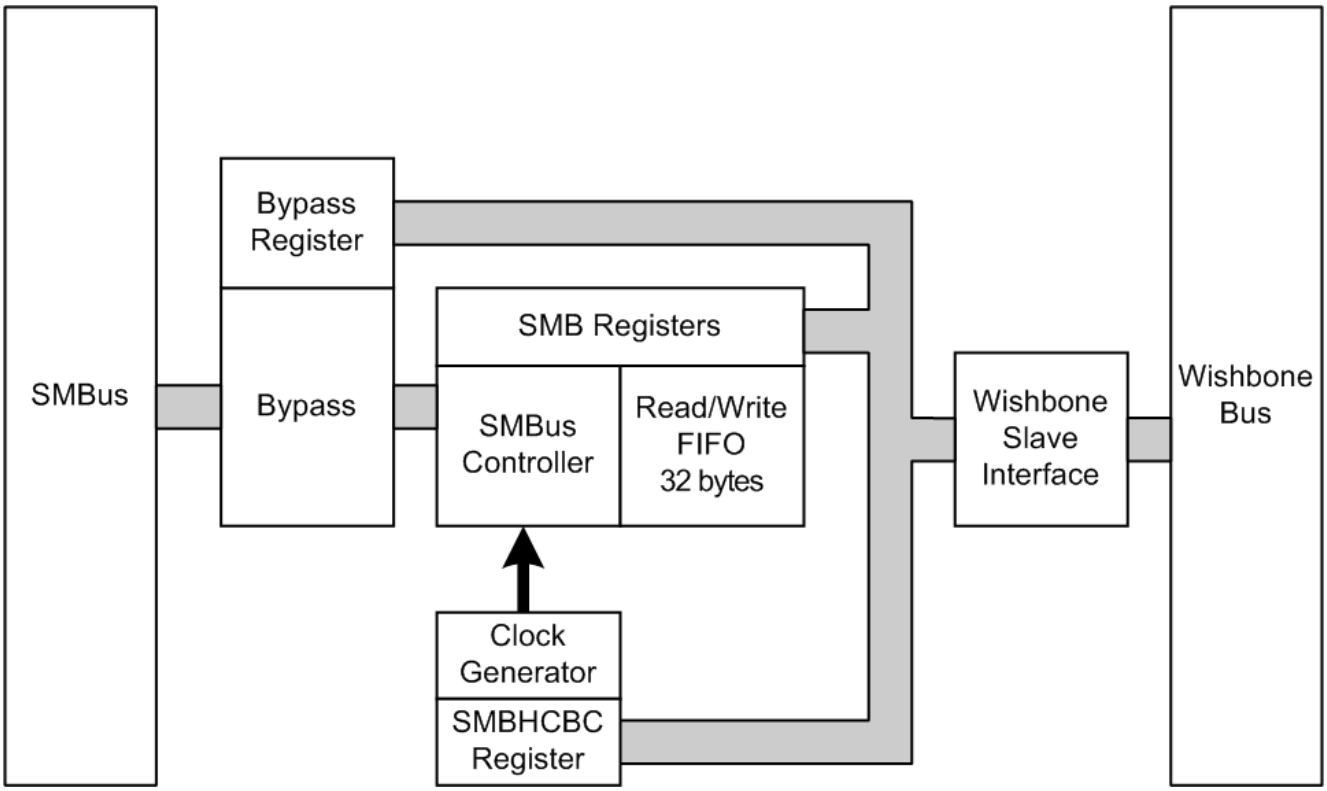
Diagram


SMBus
Bypass Register
Bypass
SMB Registers
SMBus Controller
Read/Write FIFO 32 bytes
Clock Generator
SMBHCBC Register
Wishbone Slave Interface
Wishbone Bus

Technical Data

Size	■ Logic elements (Altera® Cyclone® device family): 550 typ. ■ Pin count: 2 ■ RAM: 1 x 4096 bits
System-Bus Interface	■ Wishbone bus interface compliant with Wishbone Specification B.3 ■ 32-bit data transfer, 33MHz bus frequency ■ Supported Wishbone bus cycles □ Single read/write
SMBus Functionality	■ Master operation (revisions 7 and later with Multi-Master support, latest software drivers required!) ■ Quick send byte ■ Quick receive byte ■ Write byte/write word ■ Read byte/read word ■ Block read/block write ■ Read/write I²C message ■ Baud rate generator ■ Interrupt

Ordering Information

Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	13Z001-90	Linux host driver (MEN) for 16Z001_SMB (I2C)
For operating systems not mentioned here contact MEN sales.		
Documentation	**22Z001-00**	16Z001_SMB Reference Manual

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