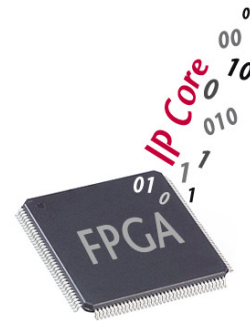


# 16Z037\_GPIO – GPIO Controller with Serial Interface IP Core

- **FPGA IP Core**
- **8 input/output ports via serial SPI interface**
- **Separate programmable interrupts for each input**
- **Wishbone bus interface**

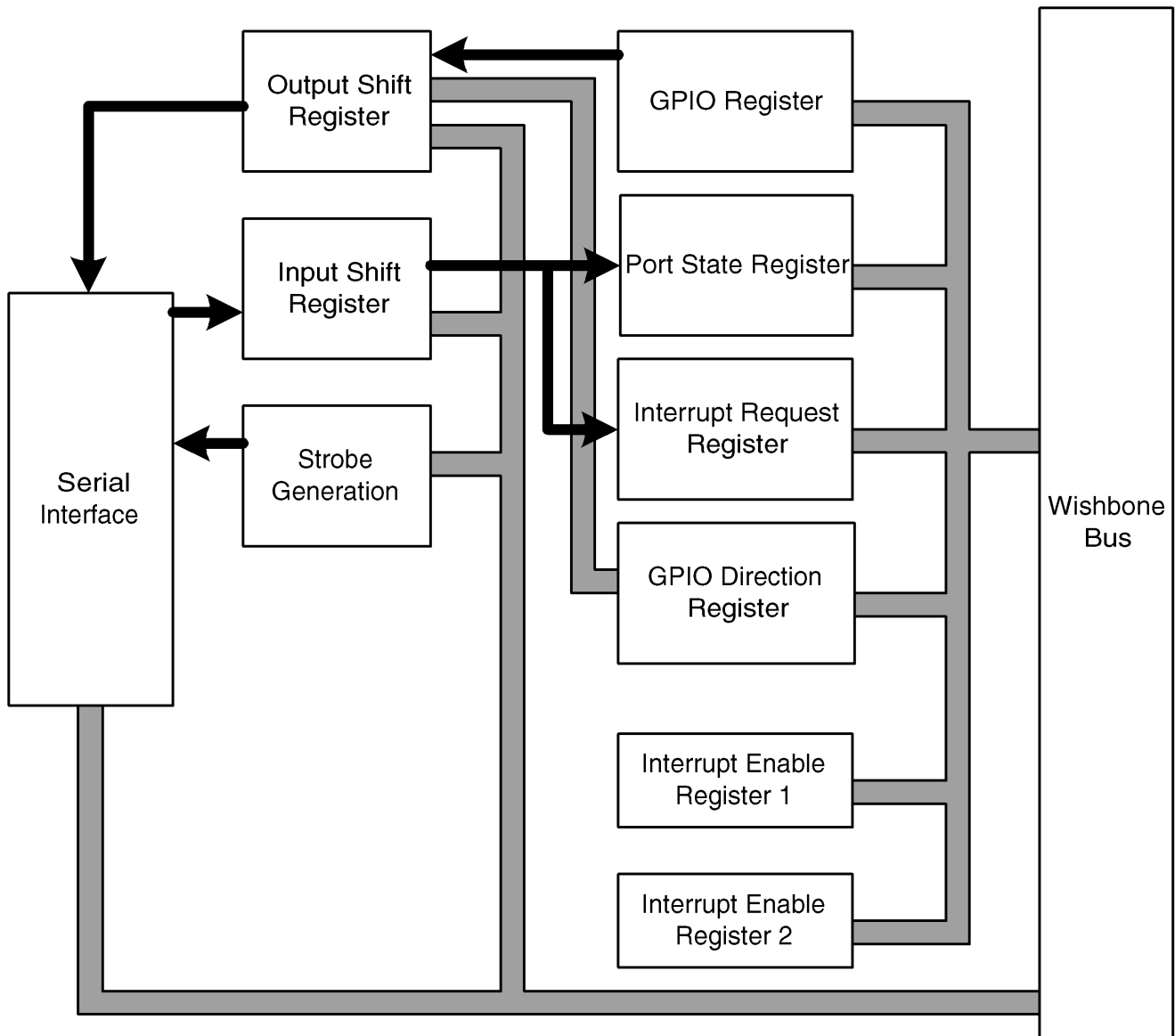
This functional block is a General Purpose Input/Output core with 8 input/output ports via a serial SPI interface. The core is able to generate separate interrupts for each input. The usage of a pin can be set in a GPIO Direction Register. Two Interrupt Enable Registers give the possibility to set the edge of the input signal (rising, falling or both) which shall generate an interrupt. The state of the GPIO input pins can be read with the Port State Register.

MEN IP cores are described in standard VHDL language and the standard Wishbone bus is used as the system interface.



By using IP cores, application-specific functions can be performed flexibly and individually in the FPGA on a growing range of MEN CPU boards. These IP cores can be assembled from the MEN function library and reconfigured, combined with IP cores from other providers or even completely redeveloped as required. The FPGA behaves just like a standard PCI component. The FPGA functions are loaded by software when the system is booted and are available in less than 1 s. On PowerPC® platforms the FPGA can be dynamically updated during operation. On Pentium® platforms FPGA updates are also possible in the boot Flash during operation and are then available once the system is rebooted.

## Diagram



## Technical Data

<b>Size</b>	<ul style="list-style-type: none"> <li>■ Logic elements (Altera® Cyclone® device family): 120 typ.</li> <li>■ Pin count: 4</li> </ul>
<b>System-Bus Interface</b>	<ul style="list-style-type: none"> <li>■ Wishbone bus interface compliant with Wishbone Specification B.3</li> <li>■ 8-bit data transfer, 66MHz bus frequency</li> <li>■ Supported Wishbone bus cycles <ul style="list-style-type: none"> <li>□ Single read/write</li> </ul> </li> </ul>
<b>GPIO Functionality</b>	<ul style="list-style-type: none"> <li>■ Up to 8 general purpose input/output ports</li> <li>■ Interrupt on input signal change (rising and/or falling edge)</li> <li>■ Separate programmable interrupts for each input</li> <li>■ Re-readable outputs</li> <li>■ Generics for all register values</li> </ul>

## Ordering Information

<b>Software: Linux</b>	<p>This product is designed to work under Linux. See below for potentially available separate software packages from MEN.</p> <p><b>13Z017-06</b>      MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</p>
<b>Software: VxWorks®</b>	<p>This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.</p> <p><b>13Z017-06</b>      MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</p>
<b>Software: QNX®</b>	<p>This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.</p> <p><b>13Z017-06</b>      MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</p>
<b>Software: OS-9®</b>	<p>This product is designed to work under OS-9®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.</p> <p><b>13Z017-06</b>      MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</p>

For operating systems not mentioned here [contact MEN sales](#).

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