

16Z055_HDLC – Single-Channel HDLC Controller IP Core

- **FPGA IP Core**
- **One HDLC channel**
- **Baud rate range from 9600 bit/s up to 1 Mbit/s**
- **Wishbone bus interface**

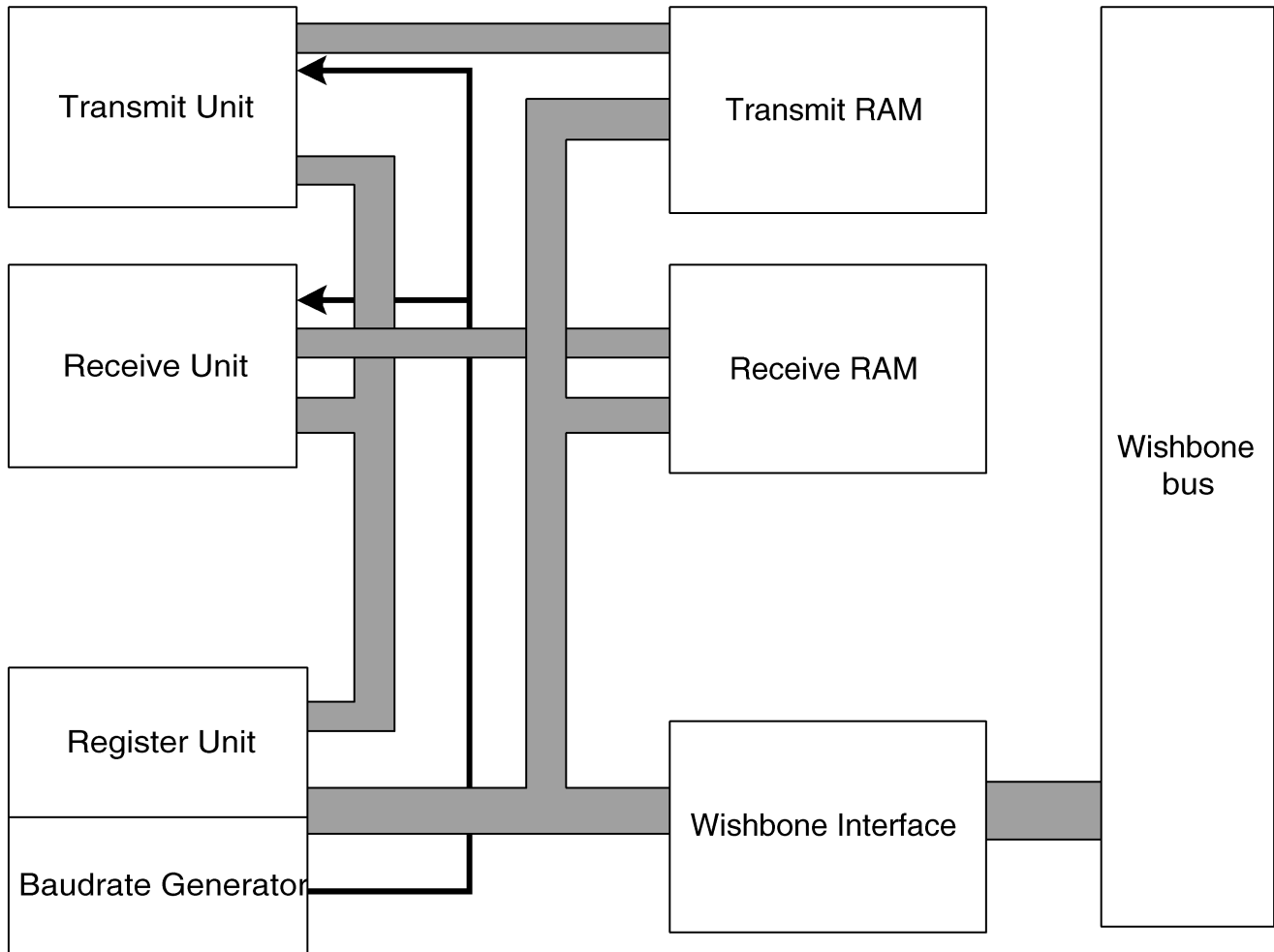
The HDLC Controller is a VHDL core with wishbone interface. One HDLC channel is included. An alternating buffer is implemented both for transmitter and receiver for data storage. With a generate option, the size of the buffer can be set in the VHDL code. The default memory size of the transfer buffer is 2 kB. One transfer buffer contains always only one frame. The baudrate can be set in ranges from 9600 bit/s up to 1 Mbit/s.

MEN IP cores are described in standard VHDL language and the standard Wishbone bus is used as the system interface.



By using IP cores, application-specific functions can be performed flexibly and individually in the FPGA on a growing range of MEN CPU boards. These IP cores can be assembled from the MEN function library and reconfigured, combined with IP cores from other providers or even completely redeveloped as required. The FPGA behaves just like a standard PCI component. The FPGA functions are loaded by software when the system is booted and are available in less than 1 s. On PowerPC® platforms the FPGA can be dynamically updated during operation. On Pentium® platforms FPGA updates are also possible in the boot Flash during operation and are then available once the system is rebooted.

Diagram



Technical Data

Size	<ul style="list-style-type: none">■ Logic elements (Altera® Cyclone® device family): 1050 typ.■ Pin count: 6■ RAM: 16 x 4096 bits
System-Bus Interface	<ul style="list-style-type: none">■ Wishbone bus interface compliant with Wishbone Specification B.3■ 32-bit data transfer, 33MHz bus frequency■ Supported Wishbone bus cycles<ul style="list-style-type: none">□ Single read/write
HDLC Functionality	<ul style="list-style-type: none">■ One HDLC channel■ Alternating buffer for data storage (2 kB default memory size)■ Baud rate range 9600 bit/s up to 1 Mbit/s■ Full duplex mode■ Handshake (RTS, CTS, DTR and DSR support in software flow control)■ CRC: CCITT ($x^{16} + x^{12} + x^5 + 1$)■ Coding: Manchester or NRZI-Manchester

Ordering Information

Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN. 13Z055-90 Linux native driver (MEN) for 16Z055_HDLC with TCP/PPP support
Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets. 13Z055-40 QNX® native driver (MEN) for 16Z055_HDLC

For operating systems not mentioned here [contact MEN sales](#).

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