

16Z042_LPC – LPC to Wishbone Bridge IP Core

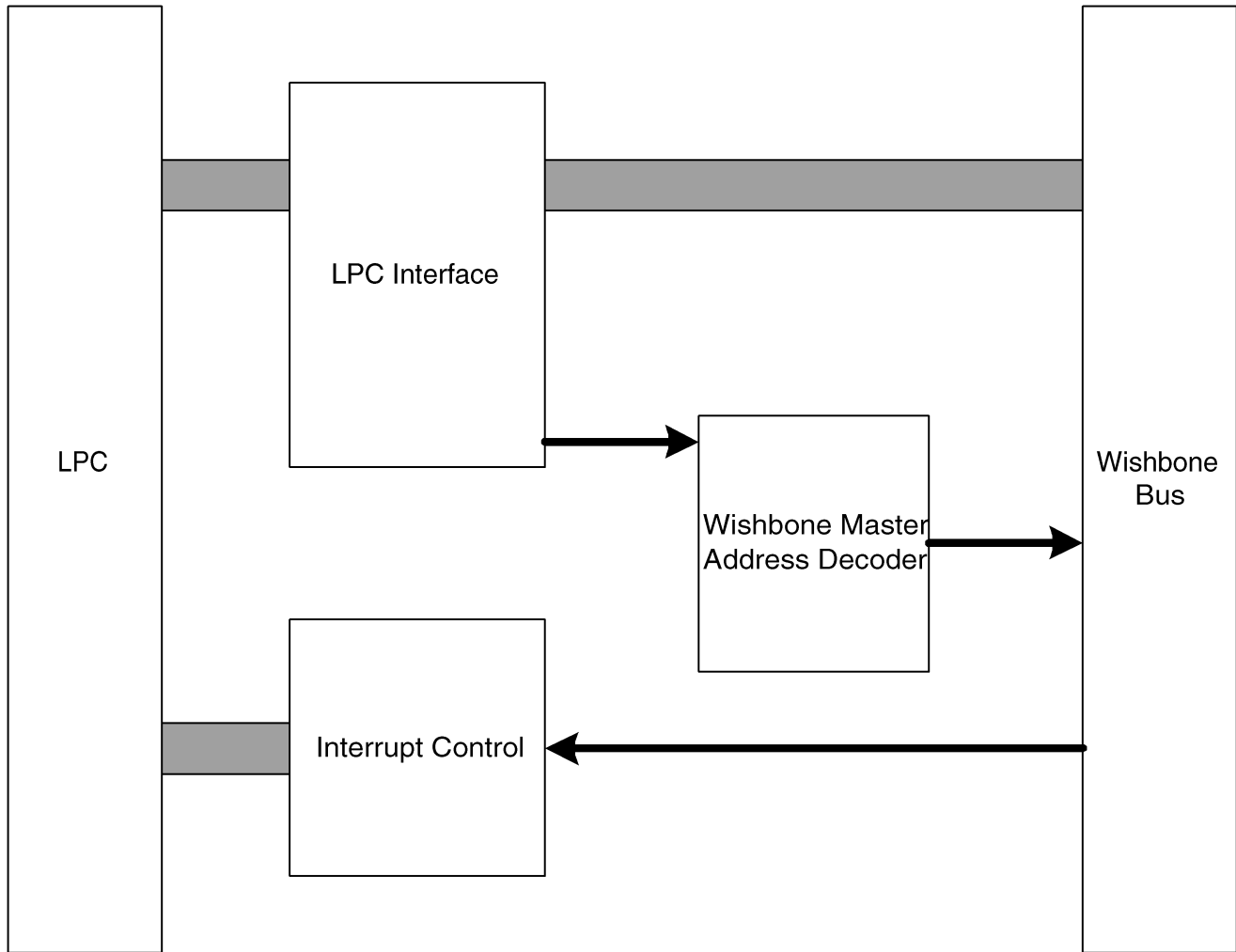
- **FPGA IP core**
- **Wishbone bus interface**
- **Conversion of LPC bus accesses**

The LPC to Wishbone Bridge is used to convert LPC bus accesses from an I/O controller to the wishbone bus internally used in the FPGA. It can be used to access standard interfaces like serial interfaces, floppy disk controller or parallel ports. The LPC to Wishbone Bridge supports I/O read, I/O write, memory read and memory write accesses in byte mode. The LPC to Wishbone bridge can be used to access the COM ports in Embedded System Modules(ESMs), for example. MEN IP cores are described in standard VHDL language and the standard Wishbone bus is used as the system interface.

By using IP cores, application-specific functions can be performed flexibly and individually in the FPGA on a growing range of MEN CPU boards. These IP cores can be assembled from the MEN function library and reconfigured, combined with IP cores from other providers or even completely redeveloped as required. The FPGA behaves just like a standard PCI component. The FPGA functions are loaded by software when the system is booted and are available in less than 1 s. On PowerPC® platforms the FPGA can be dynamically updated during operation. On Pentium® platforms FPGA updates are also possible in the boot Flash during operation and are then available once the system is rebooted.



Diagram



Technical Data

Size	<ul style="list-style-type: none">■ Logic elements (Altera® Cyclone® device family): 260 typ.■ Pin count: 13
System-Bus Interface	<ul style="list-style-type: none">■ Wishbone bus interface compliant with Wishbone Specification B.3■ 32-bit data transfer, 33MHz bus frequency■ Supported Wishbone bus cycles<ul style="list-style-type: none">□ Single read/write■ Access to up to 8 Wishbone slaves
LPC Functionality	<ul style="list-style-type: none">■ LPC Slave interface■ No LPC bus master functionality support■ Access to serial interfaces, floppy disk controller, parallel ports■ Access to COM ports in Embedded System Modules■ Memory read/write and I/O read/write operations■ Byte mode■ No DMA support

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