

16Z087_ETH – Ethernet MAC IP Core

- **FPGA IP Core**
- **10/100Base-T Ethernet support**
- **MAC layer functions**

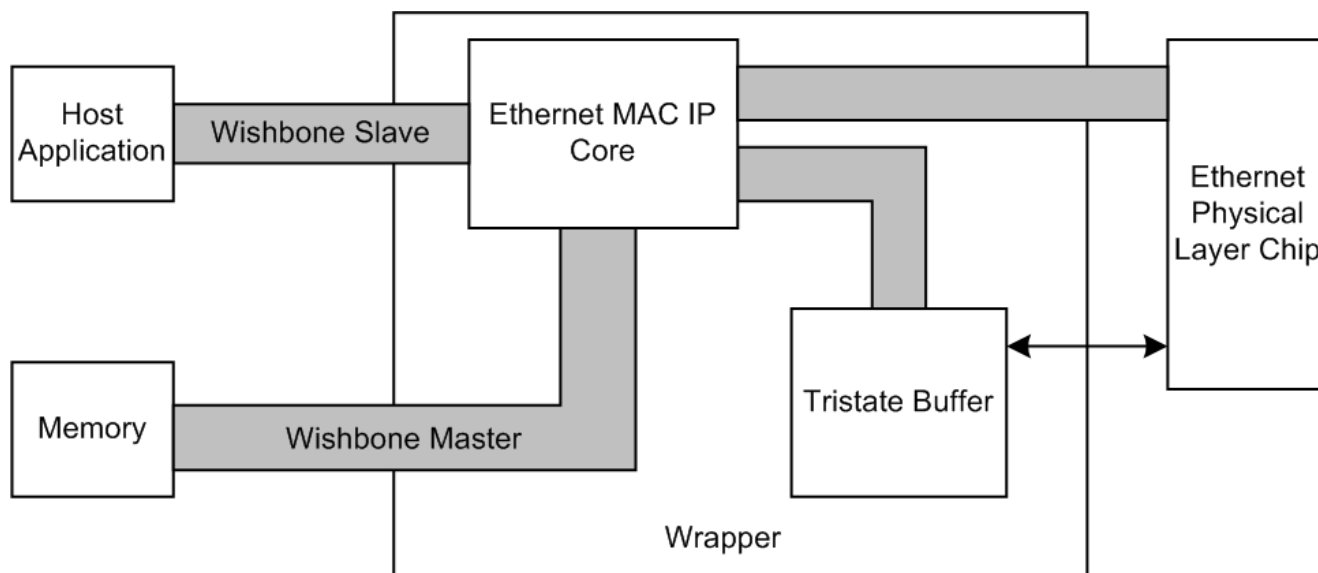


This Fast Ethernet IP core allows communication between an external physical Ethernet chip and a host application. The Wishbone master is able to read or write the data for transmitting or receiving from or into a defined memory space. This IP core has got a master and a slave Wishbone interface.

MEN IP cores are described in standard VHDL language and the standard Wishbone bus is used as the system interface.

By using IP cores, application-specific functions can be performed flexibly and individually in the FPGA on a growing range of MEN CPU boards. These IP cores can be assembled from the MEN function library and reconfigured, combined with IP cores from other providers or even completely redeveloped as required. The FPGA behaves just like a standard PCI component. The FPGA functions are loaded by software when the system is booted and are available in less than 1 s. On PowerPC® platforms the FPGA can be dynamically updated during operation. On Pentium® platforms FPGA updates are also possible in the boot Flash during operation and are then available once the system is rebooted.

Diagram



Technical Data

Size	<ul style="list-style-type: none"> ■ Logic elements (Altera® Cyclone® device family): 3400 typ. ■ Pin count min.: 14 (without half duplex and error signal) ■ Pin count typ.: 18 ■ RAM: 9 x M4K (Cyclone® I and II) or 5 x M9K (Cyclone® III)
System-Bus Interface	<ul style="list-style-type: none"> ■ Wishbone bus interface compliant with Wishbone Specification B.3 ■ 32-bit data transfer, up to 125 MHz bus frequency ■ Supported Wishbone bus cycles (master) <ul style="list-style-type: none"> □ Single read/write □ Burst read/write ■ Supported Wishbone bus cycles (slave) <ul style="list-style-type: none"> □ Single read/write
Ethernet Functionality	<ul style="list-style-type: none"> ■ 10Base-T, 100Base-T, 100Base-TX ■ MAC layer functions ■ Half duplex / full duplex ■ Flow control according to IEEE 802.3x ■ 64 transmit and 64 receive buffers

Ordering Information

Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	13Z077-90	Linux native driver (MEN) for 16Z077_ETH and 16Z087_ETH
Software: Windows®	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN.	
	13Z087-70	Windows® native driver (MEN) for 16Z087_ETH (Ethernet controller)
Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z087-40	QNX® native driver (MEN) for 16Z087_ETH
For operating systems not mentioned here contact MEN sales .		
Documentation	22Z087-ER	16Z087_ETH Errata
	22Z087-00	16Z087_ETH Reference Manual

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