CoreExpress®-ECO

CoreExpress Module

Technical Manual

TME-CEM-ECO-R2V2.doc
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Technical Manual CoreExpress-ECO

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1 Overview

1.1 Introduction

The CoreExpress-ECO is an all-in-one CPU module. The system's main memory is soldered down on the board, providing 2Gbyte, 1Gbyte or 512 Mbyte DDR2 SDRAM. Other features are two PCI-Express x1 lanes, eight USB 2.0 compliant ports, SDVO interface, High Definition Audio port, PATA interface, SD/SDIO/MMC interface, LPC Bus, SMB Bus and LVDS interface with backlight control. All interfaces are located on the high pin count module connector.

At the core of the board works the Intel® Atom™ processor at 1.6 GHz or 1.1 GHz together with the Intel® System Controller Hub chipset featuring a high performance graphics controller with 2D and 3D support. All different kinds of display interfaces like VGA, DVI, HDMI can be realized using the SDVO port and external transmitters. TFT-Panels can be handled via 24 Bit LVDS. The 64 Bit wide memory controller is integrated in the chipset providing low latency and an operating frequency of up to 266 MHz, 533 MT/S for DDR2 (Double Data Rate).

The Intel® System Controller Hub chipset provides the basic PC infrastructure of the board. and incorporates many I/O functions. The device contains state-of-the-art power management that enables systems to significantly reduce power consumption.

The module comes with an integrated microcontroller that implements LiPPERT Enhanced Management Technology (LEMT) functions. Among other things, these functions are all for condition monitoring of the device.

Features

CPU

- Intel Atom 1.6 GHz or 1.1 GHz

Main Memory

- Standard versions: 2 GByte of soldered DDR2 SDRAM
  1 GByte of soldered DDR2 SDRAM
  512 MByte of soldered DDR2 SDRAM

Chipset

- Intel System Controller Hub

Extension slots

- CoreExpress™ module connector

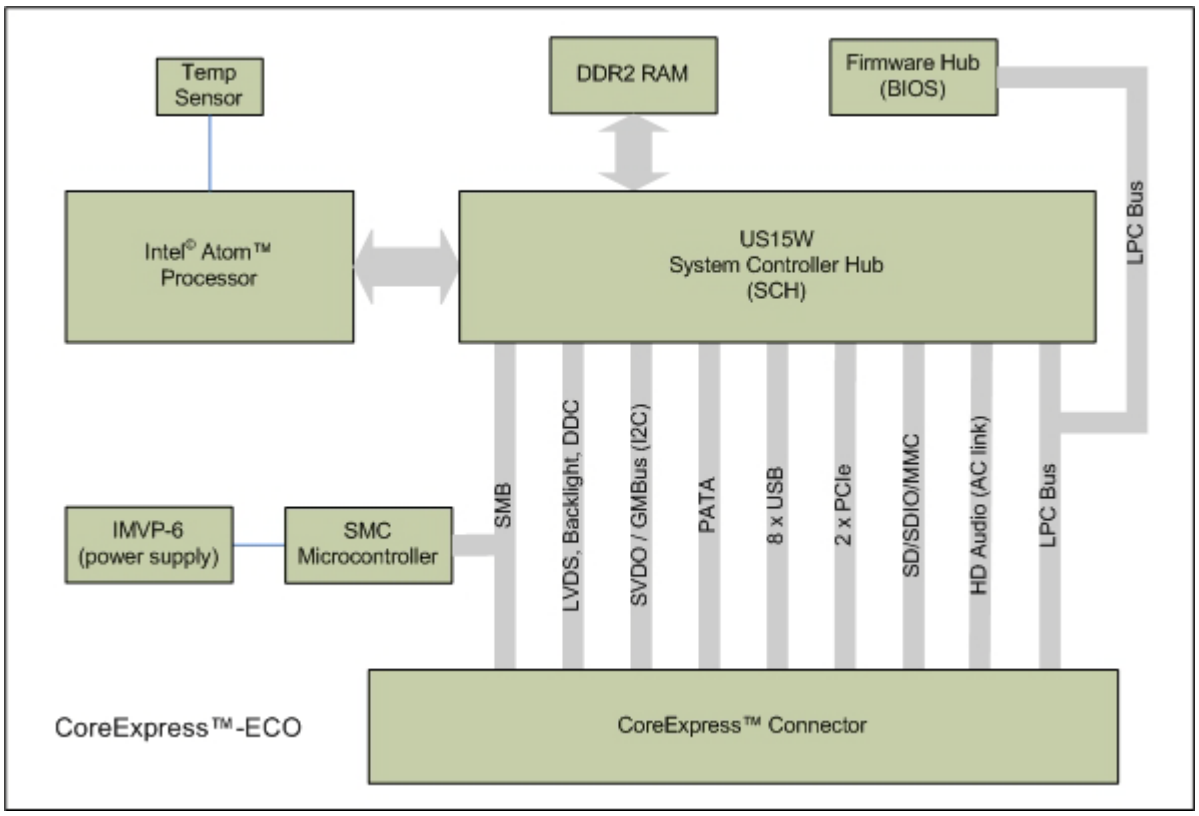
Interfaces

- 2 x PCI-Express x1 lanes
- ATA/ATAPI-6 EIDE (Ultra DMA/100)
- 8 x USB 2.0 ports
- USB port 2 can work as USB client
- LowPinCount Bus
- System Management Bus
- Intel High Definition Audio Interface
- SDVO port
- 24 Bit LVDS for displays
- backlight control signals
- SD/SDIO/MMC 4 Bit interface

Other Features

- Onboard Microcontroller with LEMT (Lippert Enhanced Management Technology)
- Onboard Power supply for all necessary voltages
- Single 5 V power supply

Block Diagram



1.2 Compatibility to SFF-SIG CoreExpress specification

The CoreExpress-ECO was developed in accordance with the original CoreExpress specification, defined and introduced by LiPPERT Embedded Computers in 2008.

In 2009 LiPPERT Embedded Computers decided to make the CoreExpress specification into an open standard under control of SFF-SIG. This move should give other companies the opportunity to design their own CoreExpress modules, enabling customer advantages due to improved availability and a broader spectrum of CoreExpress modules.

A new CoreExpress specificaton was finally adopted by the SFF-SIG as an open standard in March 2010.

During the adoption process the CoreEpxress specification has been revised by a joint technical working group. It suggested several improvements to the original specification, to cover future CPUs and chipsets from different silicon vendors. Changes proposed concerned the functionality of some pins of the CoreExpress connector resulting in minor pin function differences. These differences only affect the pins used for the IDE port, which originally has been an alternative pin usage to the SATA interface.

The SFF-SIG CoreEpress specification disposed of the alternative IDE port; it only uses the SATA interface.

The affected pins are marked in the pin assignment section of this manual.

Some other changes to the original specification refer to interfaces or pins not used by CoreExpress-ECO anyway, thus having no effect on existing custom carrier boards.

Consequently, there should be no compatibility issues for customer who already designed CoreExpress-ECO baseboards, provided they do not use the IDE ports.

1.3 Ordering Information

CoreExpress-ECO Models

Order number	Description
813-0002-10	CoreExpress-ECO module with Intel® Atom™™ Z530 processor (1.6 GHz) and 1GB DDR2 RAM onboard. Operating temperature range: -20°C .. +60°C
813-0004-10	CoreExpress-ECO module with Intel® Atom™™ Z510 processor (1.1 GHz) and 1GB DDR2 RAM onboard Operating temperature range: -20°C .. +60°C
913-0002-10	CoreExpress-ECO module with Intel® Atom™ Z530 processor (1.6 GHz) and 1GB DDR2 RAM onboard. Operating temperature range: -40°C .. +85°C
913-0004-10	CoreExpress-ECO module with Intel® Atom™ Z510 processor (1.1 GHz) and 1GB DDR2 RAM onboard. Operating temperature range: -40°C .. +85°C

Note: Custom combinations of processor and memory are possible.
Minimum order quantities are required.
Contact LiPPERT's Sales Team at sales@lippertembedded.com

Accessories

There are accessories available for CoreExpress-ECO. Please check their availability before ordering.

Order number	Description
865-0020-10	Heat sink, passive, CoreExpress-ECO
808-0005-10	CoreExpress-ECO Evaluation Kit with CoreExpress-ECO module (1.6GHz, 1GB RAM), EPIC CoreExpress-ECO carrier and pre-installed Windows XP Embedded Evaluation Version BSP (on CFD).
808-0006-10	CoreExpress-ECO Evaluation Kit with CoreExpress-ECO module (1.6GHz, 1GB RAM), EPIC CoreExpress-ECO carrier and pre-installed Linux BSP (on CFD).

1.4 Specifications

Electrical Specifications

Supply voltage	+5 V DC
Rise time	< 10 ms
Supply voltage ripple	± 3%
Inrush current	typ. 1 A
Supply	5 V
Z530 CPU (1.6 GHz):	max. 6.75 W, depending on operating system typ. 5 W.
Z510 CPU (1.1 GHz):	max. 6.25 W, depending on operating system typ. 4.5 W.
Battery voltage (BAT_IN)	+2.5 to +3.6 V DC
Battery current (BAT_IN)	5 µA (typically)

Environmental Specifications

Operating:

Temperature range	-20 °C … 60 °C (standard version)
	-40 °C … 85 °C (extended version)
Temperature change	max. 10K / 30 minutes
Humidity (relative)	10 … 90 % (non-condensing)
Pressure	450 … 1100 hPa

Non-Operating / Storage / Transport:

Temperature range	-40 °C … 85 °C
Temperature change	max. 10K / 30 minutes
Humidity (relative)	5 … 95 % (non-condensing)
Pressure	450 … 1100 hPa

MTBF

MTBF at 25°C	340.709 hours

In order to perform a failure rate assessment, several assumptions have to be made to minimize the complexity of the analysis.

Basis for the calculation was „Parts-Stress“ method according to MIL-HDBK-217 F Notice 2. Although this method requires stress values for all components, mean stress values have been used.

Environmental factor „Ground Benign“ according to MIL-HDBK-217 has been used as well as an environmental temperature of 25 °C.

Failure rate of mechanical components (screws, chassis, etc) is negligible.

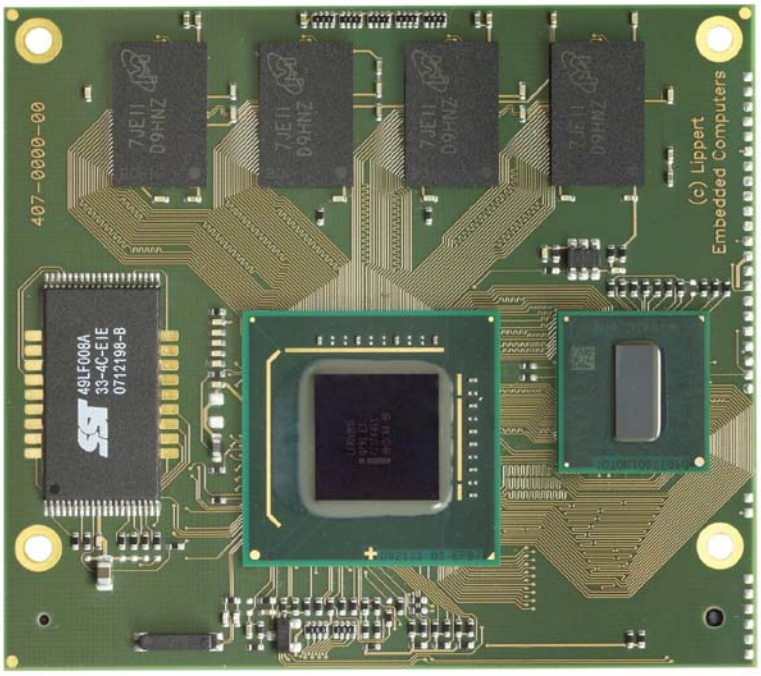
Mechanical

Dimensions (LxW)	65 mm x 58 mm
Height	max. 2.1 mm on topside above PCB
	max. 4.2 mm on bottom side below PCB
Weight	28 grams
Mounting	4 mounting holes for PCB, recommended diameter 2.2 mm, recommended pad size of the mounting hole or clearance around the mounting hole 5.00 mm

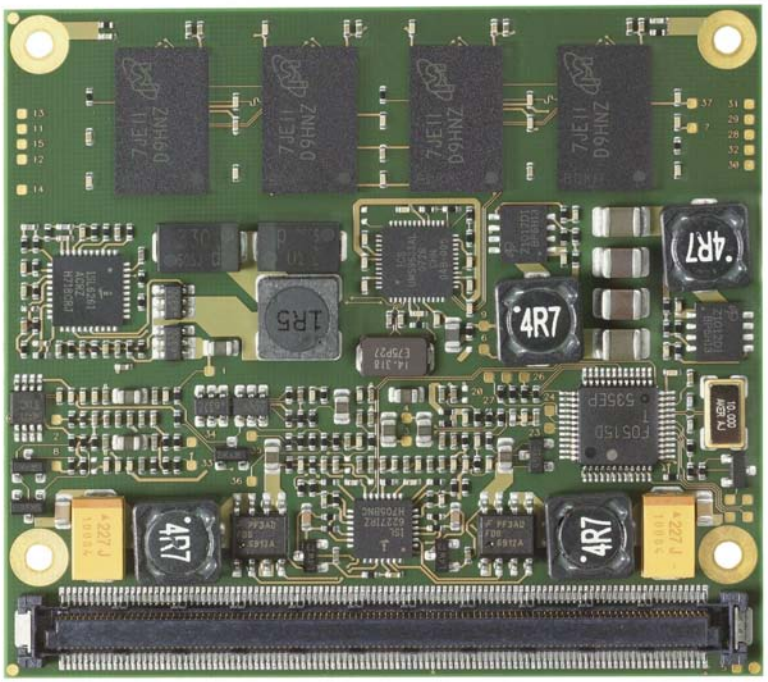
2 Getting Started

2.1 Module View

Top

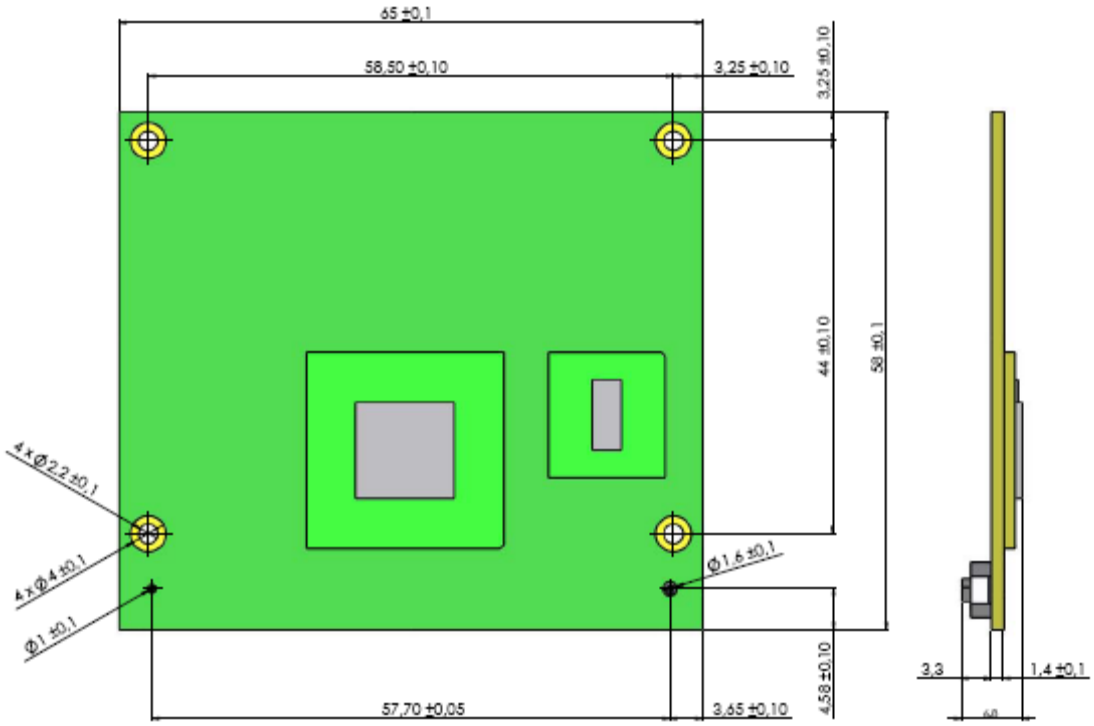


Bottom

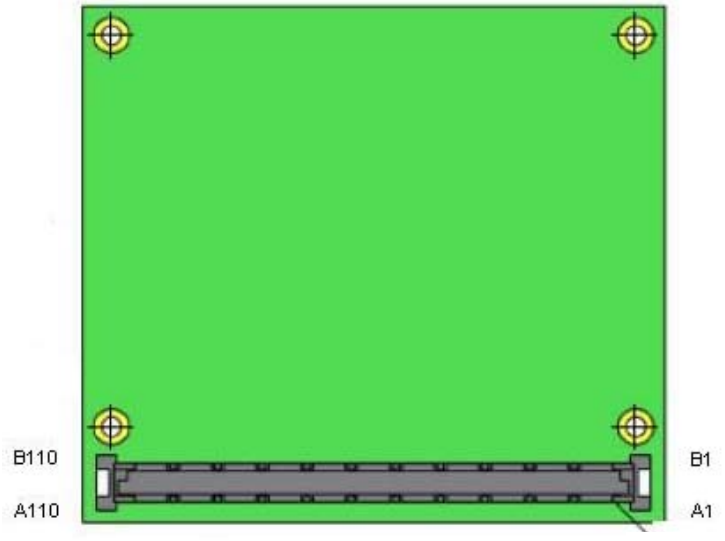


2.2 Mechanical View

Top (all dimensions are in mm)



Bottom



Pin A1

2.3 Mounting

The module is mounted on a baseboard by using metric spacers M2 male with the matching length of the baseboard connector. The standard length is 5.00 mm, optional 8.00 mm.

Caution For mounting the module hold it in parallel above the baseboard connector and press it down gently into the baseboard connector. Use four M2 screws with a length of 6 mm (assuming a baseboard thickness of 1.6 mm) to fix the module by screwing from below the baseboard.

Caution For dismounting the module, release the mounting screws and pull out the module gently from the baseboard connector. Do not bend the module to left or right. This might damage the module or baseboard connector.

2.4 Hardware Setup

Caution Be sure to follow the EMC security measures. Make sure you are always at the same potential as the module.

Caution Never connect or disconnect peripherals like HDD's while the board's power supply is connected and switched on!

Use the starter kit's EPIC carrier together with the CoreExpress-ECO module to connect a display device. Connect USB keyboard and mouse, respectively. Use the 40-wire/44-wire cable to connect the harddisk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional other peripherals, now is the time to connect them, too.

Connect a 5 volt power supply to the power connector of the baseboard and switch the power on.

Note *Please refer to the baseboard manual for the needed supply current that the power supply must provide to power the module, the baseboards and the standard peripherals. If you want to use more and/or other peripherals, please plan your power budget first! The system will not work if there is not enough supply current for all your devices.*

The display shows the BIOS messages. If you want to change the standard BIOS settings, press <DEL> at startup to enter the BIOS menu.

If you need to load the BIOS default values, press the <Insert> key during startup. This forces the BIOS to load the factory settings from FlashPROM.

CoreExpress-ECO boots from CD drives, USB floppy, USB stick, or harddisk. Provided that any of these is connected and contains a valid operating system image, the display should show the boot screen of your operating system.

Note *Not all USB devices are suitable to boot the CoreExpress-ECO from. If there are problems, please use another device from another manufacturer.*

3 Module Description

3.1 Processor

The Atom processor is built on 45-nanometer process technology — the first generation of low-power IA-32 microarchitecture. The Atom supports the Intel System Controller Hub chipset, a single-chip component design for low-power, System Controller Hub (SCH).

Major Features

The following list provides some of the key features on this processor:

- New single-core processor for mobile devices with enhanced performance
- On die, primary 32-kB instructions cache and 24-kB write-back data cache
- 100-MHz and 133-MHz Source-Synchronous front side bus (FSB)
- Supports Hyper-Threading Technology 2-threads
- On die 512-kB, 8-way L2 cache
- Support for IA 32-bit and Intel® 64 architecture
- Intel® Virtualization Technology (Intel® VT)
- Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3) support
- Supports new CMOS FSB signaling for reduced power
- Micro-FCBGA8 packaging technologies
- Thermal management support via TM1 and TM2
- FSB Lane Reversal for flexible routing
- Supports C0/C1(e)/C2(e)/C4(e)
- New C6 Deep Power Down Technology
- L2 Dynamic Cache Sizing
- New Split-VTT support for lowest processor power state
- Advanced power management features including Enhanced Intel®SpeedStep® Technology
- Execute Disable Bit support for enhanced security

3.2 System Controller Hub

The System Controller Hub (SCH) is designed for use with Atom processor-based platforms. The SCH connects directly to the processor. It incorporates a variety of PCI functions:

- Host Bridge
- Integrated Graphics and Video Device
- USB Client
- Intel® High Definition Audio (Intel® HD Audio) Controller
- PCI Express Port 1
- PCI Express Port 2
- USB Classic UHCI Controller 1
- USB Classic UHCI Controller 2
- USB Classic UHCI Controller 3
- USB2 EHCI Controller

- SDIO/MMC Port
- LPC Interface
- PATA Controller

Processor Interface

The System Controller Hub supports the Atom processor subset of the Enhanced Mode Scalable Bus Protocol, and implements a low-power CMOS bus. The SCH supports a single bus agent with FSB data rates of 400 MT/s and 533 MT/s. Its features include:

- Atom processor support
- CMOS frontside bus signaling for reduced power
- 400 MT/s or 533 MT/s data rate operation
- 64-Byte cache-line size
- 64-bit data bus, 32-bit address bus
- Supports one physical processor attachment with up to two logical processors
- 16 deep IOQ
- 1 deep defer queue
- FSB interrupt delivery
- Power-saving sideband control (DPWR#) for enabling/disabling processor data
- input sense amplifiers
- 1.05 V VTT operation

System Memory Controller

The System Controller Hub integrates a DDR2 memory controller with a single 64-bit wide interface. Only DDR2 memory is supported. The memory controller interface is fully configurable through a set of control registers. Features of the System Controller Hub memory controller include:

- Supports 1.8V DDR2 SDRAM, up to 2 ranks
- Supports 1.5V DDR2 SDRAM, 1 rank only
- Supports 400 MT/s and 533 MT/s data rates
- Single 64-bit wide channel
- Single command per clock (1-N) operation
- Support for a maximum of 1 GB of DRAM
- One or two rank operation
- Device density support for 512 Mb and 1024 Mb devices
- Device widths of x16
- Aggressive power management to reduce idle power consumption
- Page closing policies to proactively close pages after idle periods
- No on-die termination (ODT) support
- Supports non-terminated and board-terminated bus topologies

USB Host

The System Controller Hub contains three Universal Host Controller Interface (UHCI) USB 1.1 controllers and an Enhanced Host Controller Interface (EHCI) USB 2.0 controller. Portrouting logic on the system controller hub determines which USB controller is used to operate a given USB port.

A total of eight USB ports are supported. All eight of these ports are capable of highspeed data transfers up to 480MB/s, and six of the ports are also capable of full-speed and low-speed signaling. The two high-speed-only USB ports may only be used internally within the system platform.

USB Client

The System Controller Hub supports USB client functionality on port C of the USB interface. This permits the platform to attach to a separate USB host as a peripheral mass storage volume or RNDIS device.

PCI Express

The System Controller Hub has two PCI Express root ports supporting the PCI Express Base Specification, Revision 1.0a. PCI Express root ports 1–2 can be statically configured as two x1 lanes. Each root port supports 2.5 GB/s bandwidth in each direction. An external graphics device can be used via one of the x1 PCI Express lanes/ports.

LPC Interface

The System Controller Hub implements an LPC interface as described in the LPC 1.1 Specification. The LPC interface has three PCI-based clock outputs that may be provided to different I/O devices, such as Firmware Hub flash memory or a legacy I/O chip. The LPC_CLKOUT signals run at 33 MHz frequency and support a total of six loads (two loads per clock pair) with no external buffering.

Parallel ATA (PATA)

The PATA Host Controller supports three types of data transfers:

- Programmed I/O (PIO): Processor is in control of the data transfer.
- Multi-word DMA (ATA-5): DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 66MB/s.
- Ultra DMA: Synchronous DMA protocol that redefines signals on the PATA cable to allow both host and target throttling of data and transfer rates up to 100MB/s. Ultra DMA 100/66/33 are supported.

Intel Graphics Media Accelerator 500

The System Controller Hub provides integrated graphics (2D and 3D) and high-definition video decode capabilities with minimal power consumption.

Graphics

The highly compact integrated graphic device contains an advanced shader architecture (model 3.0+) that performs pixel shading and vertex shading within a single hardware accelerator. The processing of pixels is deferred until they are determined to be visible, which minimizes access to memory and improves render performance.

Video

The System Controller Hub supports full hardware acceleration of video decode standards such as H.264, MPEG2, MPEG4, VC1, and WMV9.

Display Interfaces

The integrated graphic device includes LVDS and Serial DVO display ports permitting simultaneous independent operation of two displays. If external graphics is used instead of the internal graphics device, LVDS and SDVO ports will not function.

LVDS

The System Controller Hub supports a Low-Voltage Differential Signaling interface that allows the integrated graphic device to communicate directly to an on-board flat-panel display. The LVDS interface supports pixel color depths of 18 and 24 bits.

Serial DVO (SDVO) Display

The System Controller Hub has a digital display channel capable of driving SDVO adapters (ADD2-N) that provide interfaces to a variety of external display technologies (e.g. DVI, TV-Out, analog CRT). SDVO lane reversal is not supported.

Secure Digital I/O (SDIO) / Multimedia Card (MMC) Controller

The System Controller Hub contains a SDIO/MMC expansion port used to communicate with a variety of internal or external SDIO and MMC devices. The port supports SDIO Revision 1.1 and MMC Revision 4.0 and is backward-compatible with previous interface specifications.

SMBus Host Controller

The System Controller Hub contains an SMBus host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices. The system controller hub SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). See System Management Bus (SMBus) Specification, Version 1.0.

Intel High Definition Audio (Intel® HD Audio) Controller

The Intel High Definition Audio Specification defines a digital interface that can be used to attach different types of codecs (such as audio and modem codecs). The HD Audio controller supports up to four audio streams, two in and two out. With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz, the High Definition Audio (HD Audio) controller provides audio quality that can deliver consumer electronic (CE) levels of audio experience. On the input side, the Intel® System Controller Hub adds support for an array of microphones. The Intel® HD Audio controller uses a set of DMA engines to effectively manage the link bandwidth and support simultaneous independent streams on the link. The capability enables new exciting usage models with HD Audio (e.g., listening to music while playing a multi-player game on the Internet.) The HD Audio controller also supports isochronous data transfers allowing glitch-free audio to the system.

Caution The HDA audio controller does not support standard AC97 codec devices on baseboard. A baseboard design must use a HDA audio codec.

Power Management

The System Controller Hub contains a mechanism to allow flexible configuration of various device maintenance routines as well as power management functions such as enhanced clock control and low-power state transitions (e.g., Suspend-to-RAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states. The system controller hub contains full support for the Advanced Configuration and Power Interface (ACPI) Specification, Revision 3.0.

3.3 LEMT Functions

The onboard Microcontroller implements power sequencing and LEMT (**L**iPPERT **E**nhanced **M**anagement **T**echnology) functionality. The microcontroller communicates via the System Management Bus with the CPU/Chipset. The following functions are implemented:

- Total operating hours counter
  Counts the number of hours the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature
  Min. and max. temperature values of CPU and board are stored in flash.
- Power cycles counter
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Fail-Safe-BIOS Support
  In case of a Boot failure, hardware signals tells external logic to boot from a Fail-Safe-BIOS.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can stored in a write- and clear-protectable region.
- Manufacturing information
  Part number / Serial number / BIOS version / Test date

4 CoreExpress Connector

4.1 Pin Assignment

The CoreExpress connector holds all interface signals to be used on the baseboard. Due to the available chipset interfaces CoreExpress-ECO supports only a subset of the CoreExpress specification. All unused signal are marked as ***reserved for future use*** in this list. The systems designer must not connect any signal to those pins, other than for the purpose stated in the CoreExpress specification.

Connector Type: TYCO 3-6318490-6 or equivalent

Pin#	Signal Name	Bus	Voltage Level	Diff. Sig.
A1	GND	POWER	0V	no
A2	PCIE_TXAn	PCIExpress	AC coupled	yes
A3	PCIE_TXAp	PCIExpress	AC coupled	yes
A4	PCIE_CLKAn	PCIExpress	3.3V	yes
A5	PCIE_CLKAp	PCIExpress	3.3V	yes
A6	GND	POWER	0V	no
A7	PCIE_TXBn	PCIExpress	AC coupled	yes
A8	PCIE_TXBp	PCIExpress	AC coupled	yes
A9	*reserved for future use*			
A10	*reserved for future use*			
A11	GND	POWER	0V	no
A12	*reserved for future use*			
A13	*reserved for future use*			
A14	*reserved for future use*			
A15	*reserved for future use*			
A16	GND	POWER	0V	no
A17	CLKREQA#	PCIExpress	3.3V	no
A18	*reserved for future use*			
A19	SDVOB_CLK#	SDVO	AC coupled	yes
A20	SDVOB_CLK	SDVO	AC coupled	yes
A21	GND	POWER	0V	no
A22	SDVOB_GREEN	SDVO	AC coupled	yes
A23	SDVOB_GREEN#	SDVO	AC coupled	yes
A24	SDVOB_TVCLKIN#	SDVO	AC coupled	yes
A25	SDVOB_TVCLKIN	SDVO	AC coupled	yes
A26	GND	POWER	0V	no
A27	SDVOB_RED	SDVO	AC coupled	yes
A28	SDVOB_RED#	SDVO	AC coupled	yes
A29	LA_DATA0p	LVDS	Low voltage	yes
A30	LA_DATA0n	LVDS	Low voltage	yes
A31	GND	POWER	0V	no
A32	LA_DATA2p	LVDS	Low voltage	yes
A33	LA_DATA2n	LVDS	Low voltage	yes

Pin#	Signal Name	Bus	Voltage Level	Diff. Sig.
A34	LA_DATA3p	LVDS	Low voltage	yes
A35	LA_DATA3n	LVDS	Low voltage	yes
A36	GND	POWER	0V	no
A37	L_DDC_DATA	LVDS	3.3V	no
A38	L_DDC_CLK	LVDS	3.3V	no
A39	USB_Ap	USB2.0	Low voltage	yes
A40	USB_An	USB2.0	Low voltage	yes
A41	GND	POWER	0V	no
A42	USB_Cp	USB2.0	Low voltage	yes
A43	USB_Cn	USB2.0	Low voltage	yes
A44	USB_Ep	USB2.0	Low voltage	yes
A45	USB_En	USB2.0	Low voltage	yes
A46	GND	POWER	0V	no
A47	USB_Gp	USB2.0	Low voltage	yes
A48	USB_Gn	USB2.0	Low voltage	yes
A49	USB_A/B_OC#	USB2.0	3.3V	no
A50	USB_E/F_OC#	USB2.0	3.3V	no
A51	GND	POWER	0V	no
A52	*reserved for future use*			
A53	*reserved for future use*			
A54	*reserved for future use*			
A55	*reserved for future use*			
A56	SMB_CLK	SMB	3.3V	no
A57	SMB_DATA	SMB	3.3V	no
A58	SMB_ALERT#	SMB	3.3V	no
A59	*reserved for future use*			
A60	GND	POWER	0V	no
A61	***IDE_PDD3***	***IDE***	***3.3V-5V tol.***	***no***
A62	***IDE_PDA0***	***IDE***	***3.3V-5V tol.***	***no***
A63	***IDE_PDA2***	***IDE***	***3.3V-5V tol.***	***no***
A64	***IDE_PDD8***	***IDE***	***3.3V-5V tol.***	***no***
A65	***IDE_PDDREQ***	***IDE***	***3.3V-5V tol.***	***no***
A66	***IDE_PDA1***	***IDE***	***3.3V-5V tol.***	***no***
A67	***IDE_PDD13***	***IDE***	***3.3V-5V tol.***	***no***
A68	***IDE_PDD1***	***IDE***	***3.3V-5V tol.***	***no***
A69	***INT_IRQ14***	***IDE***	***3.3V-5V tol.***	***no***
A70	GND	POWER	0V	no
A71	***IDE_PDD11***	***IDE***	***3.3V-5V tol.***	***no***
A72	***IDE_PDD5***	***IDE***	***3.3V-5V tol.***	***no***
A73	***IDE_PDIOR#***	***IDE***	***3.3V-5V tol.***	***no***
A74	***IDE_PDD14***	***IDE***	***3.3V-5V tol.***	***no***
A75	***IDE_PDCS1#***	***IDE***	***3.3V-5V tol.***	***no***
A76	LPC_AD3	LPC	3.3V	no

Pin#	Signal Name	Bus	Voltage Level	Diff. Sig.
A77	LPC_AD1	LPC	3.3V	no
A78	LPC_AD0	LPC	3.3V	no
A79	LPC_FRAME#	LPC	3.3V	no
A80	GND	POWER	0V	no
A81	SD0_WP	SDIO 8Bit	3.3V	no
A82	SD0_CD#	SDIO 8Bit	3.3V	no
A83	SD0_CLK	SDIO 8Bit	3.3V	no
A84	SD0_DATA1	SDIO 8Bit	3.3V	no
A85	SD0_DATA3	SDIO 8Bit	3.3V	no
A86	SD0_DATA5 (don´t use)	SDIO 8Bit	3.3V	no
A87	SD0_DATA6 (don´t use)	SDIO 8Bit	3.3V	no
A88	L_CTLB_DATA	LVDS	3.3V	no
A89	L_CTLB_CLK	LVDS	3.3V	no
A90	GND	POWER	0V	no
A91	HDA_DOCK_EN#	HD Audio	1.8V or 3.3V	no
A92	HDA_SDATAIN1	HD Audio	1.8V or 3.3V	no
A93	HDA_SDATAOUT	HD Audio	1.8V or 3.3V	no
A94	HDA_RST#	HD Audio	1.8V or 3.3V	no
A95	*reserved for future use*			
A96	*reserved for future use*			
A97	*reserved for future use*			
A98	*reserved for future use*			
A99	*reserved for future use*			
A100	GND	POWER	0V	no
A101	RST_OUT#	CONTROL	3.3V	no
A102	RST_IN#	CONTROL	3.3V	no
A103	WAKE#	CONTROL	3.3V	no
A104	+5V0	POWER	5V	no
A105	+5V0	POWER	5V	no
A106	+5V0	POWER	5V	no
A107	+5V0	POWER	5V	no
A108	+5V0	POWER	5V	no
A109	+5V0	POWER	5V	no
A110	GND	POWER	0V	no
B1	GND	POWER	0V	no
B2	PCIE_RXAn	PCIExpress	AC coupled	yes
B3	PCIE_RXAp	PCIExpress	AC coupled	yes
B4	PCIE_CLKBn	PCIExpress	3.3V	yes
B5	PCIE_CLKBp	PCIExpress	3.3V	yes
B6	GND	POWER	0V	no
B7	PCIE_RXBn	PCIExpress	AC coupled	yes
B8	PCIE_RXBp	PCIExpress	AC coupled	yes
B9	*reserved for future use*			

Pin#	Signal Name	Bus	Voltage Level	Diff. Sig.
B10	*reserved for future use*			
B11	GND	POWER	0V	no
B12	*reserved for future use*			
B13	*reserved for future use*			
B14	*reserved for future use*			
B15	*reserved for future use*			
B16	GND	POWER	0V	no
B17	CLKREQB#	PCIExpress	3.3V	no
B18	*reserved for future use*			
B19	SDVOB_INT#	SDVO	AC coupled	yes
B20	SDVOB_INT	SDVO	AC coupled	yes
B21	GND	POWER	0V	no
B22	SDVOB_BLUE	SDVO	AC coupled	yes
B23	SDVOB_BLUE#	SDVO	AC coupled	yes
B24	SDVOB_STALL	SDVO	AC coupled	yes
B25	SDVOB_STALL#	SDVO	AC coupled	yes
B26	GND	POWER	0V	no
B27	SDVO_CTRL_CLK	SDVO	3.3V	yes
B28	SDVO_CTRL_DAT	SDVO	3.3V	yes
B29	LA_DATA1p	LVDS	Low voltage	yes
B30	LA_DATA1n	LVDS	Low voltage	yes
B31	GND	POWER	0V	no
B32	LA_CLKp	LVDS	Low voltage	yes
B33	LA_CLKn	LVDS	Low voltage	yes
B34	L_BKLTCTL	LVDS	3.3V	no
B35	L_BKLTEN	LVDS	3.3V	no
B36	*reserved for future use*			
B37	L_VDDEN	LVDS	3.3V	no
B38	USB_C_Device	USB2.0	3.3V	no
B39	USB_Bp	USB2.0	Low voltage	yes
B40	USB_Bn	USB2.0	Low voltage	yes
B41	GND	POWER	0V	no
B42	USB_Dp	USB2.0	Low voltage	yes
B43	USB_Dn	USB2.0	Low voltage	yes
B44	USB_Fp	USB2.0	Low voltage	yes
B45	USB_Fn	USB2.0	Low voltage	yes
B46	GND	POWER	0V	no
B47	USB_Hp	USB2.0	Low voltage	yes
B48	USB_Hn	USB2.0	Low voltage	yes
B49	USB_C/D_OC#	USB2.0	3.3V	no
B50	USB_G/H_OC#	USB2.0	3.3V	no
B51	GND	POWER	0V	no
B52	*reserved for future use*			

Pin#	Signal Name	Bus	Voltage Level	Diff. Sig.
B53	*reserved for future use*			
B54	*reserved for future use*			
B55	*reserved for future use*			
B56	*reserved for future use*			
B57	*reserved for future use*			
B58	*reserved for future use*			
B59	*reserved for future use*			
B60	GND	POWER	0V	no
B61	***IDE_PDCS3#***	***IDE***	***3.3V-5V tol.***	***no***
B62	***IDE_PDDACK#***	***IDE***	***3.3V-5V tol.***	***no***
B63	***IDE_PDD4***	***IDE***	***3.3V-5V tol.***	***no***
B64	***IDE_PDD2***	***IDE***	***3.3V-5V tol.***	***no***
B65	***IDE_PDIORDY***	***IDE***	***3.3V-5V tol.***	***no***
B66	***IDE_PDD10***	***IDE***	***3.3V-5V tol.***	***no***
B67	***IDE_PDD6***	***IDE***	***3.3V-5V tol.***	***no***
B68	***IDE_PDD12***	***IDE***	***3.3V-5V tol.***	***no***
B69	***IDE_PDD9***	***IDE***	***3.3V-5V tol.***	***no***
B70	GND	POWER	0V	no
B71	***IDE_PDD15***	***IDE***	***3.3V-5V tol.***	***no***
B72	***IDE_PDD0***	***IDE***	***3.3V-5V tol.***	***no***
B73	***IDE_PDD7***	***IDE***	***3.3V-5V tol.***	***no***
B74	***IDE_PDIOW#***	***IDE***	***3.3V-5V tol.***	***no***
B75	***IDE_PATADET***	***IDE***	***3.3V***	***no***
B76	LPC_CLK_OUT2	LPC	3.3V	no
B77	LPC_CLK_OUT1	LPC	3.3V	no
B78	LPC_SERIRQ	LPC	3.3V	no
B79	LPC_AD2	LPC	3.3V	no
B80	GND	POWER	0V	no
B81	SD0_DATA7 (don´t use)	SDIO 8Bit	3.3V	no
B82	SD0_PWR#	SDIO 8Bit	3.3V	no
B83	SD0_DATA2	SDIO 8Bit	3.3V	no
B84	SD0_LED	SDIO 8Bit	3.3V	no
B85	SD0_DATA4 (don´t use)	SDIO 8Bit	3.3V	no
B86	SD0_DATA0	SDIO 8Bit	3.3V	no
B87	SD0_CMD	SDIO 8Bit	3.3V	no
B88	WDOUT	CONTROL	3.3V	no
B89	HDA_SPKR	HD Audio	3.3V	no
B90	GND	POWER	0V	no
B91	HDA_BITCLK	HD Audio	1.8V or 3.3V	no
B92	HDA_DOCK_RST#	HD Audio	1.8V or 3.3V	no
B93	HDA_SDATAIN0	HD Audio	1.8V or 3.3V	no
B94	HDA_SYNC	HD Audio	1.8V or 3.3V	no
B95	*reserved for future use*			

Pin#	Signal Name	Bus	Voltage Level	Diff. Sig.
B96	PWR_GOOD	CONTROL	3.3 V	no
B97	PS_ON	CONTROL	3.3 V	no
B98	PWRBTN#	CONTROL	3.3 V	no
B99	SUS_3#	CONTROL	3.3 V	no
B100	GND	POWER	0V	no
B101	SUS_4/5#	CONTROL	3.3 V	no
B102	BIOS_DISABLE#	CONTROL	3.3 V	no
B103	BAT_IN	POWER	2.5 – 3.6 V	no
B104	+5V0-ALWAYS	POWER	5V	no
B105	+5V0	POWER	5V	no
B106	+5V0	POWER	5V	no
B107	+5V0	POWER	5V	no
B108	+5V0	POWER	5V	no
B109	+5V0	POWER	5V	no
B110	GND	POWER	0V	no

Note *IDE Pins (bold and cursive) A61 to A75 and B61 to B75 on the CoreExpress-ECO do not conform to the SFF-SIG CoreExpress specification.*

4.2 Pin Description

Note *Name convention: All signal names ending with a # indicate a low active signal.*

Power and Ground Signal Pins

The board is powered by applying 5 volt at all these pins

+5V0: 5 volt power supply pins

+5V0-ALWAYS: 5 volt standby power supply pins for sleep and running state

GND: GND power supply pins

External Battery

An external battery (2.5 V ... 3.6 V) should be connected to the CoreExpress connector pin BAT_IN. It buffers the CMOS data for the BIOS setup and the real time clock. The supply current for BAT_IN is approx. 5 µA in buffer mode (switched off).

PCI-Express Lanes

There are two PCI Express root ports available on the CoreExpress connector. The PCI Express signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications.

The following PCI Express signals are located on the CoreExpress connector:

PCIE_TXAn, PCIE_TXAp,
PCIE_TXBn, PCIE_TXBp

Type: differential output, AC coupled

PCI Express Transmit: PCIE_TX[A:B] are PCI Express ports A:B transmit pair (P and N) signals. The serial capacitors are included on the module.

PCIE_RXAn, PCIE_RXAp,
PCIE_RXBn, PCIE_RXBp

Type: differential input, AC coupled

PCI Express Receive: PCIE_RX[A:B] PCI Express ports A:B receive pair (P and N) signals. The serial capacitors must be placed on the baseboard at the PCI Express device.

PCIE_CLKAn, PCIE_CLKAp,
PCIE_CLKBn, PCIE_CLKBp,

Type: differential output, 3.3 volt

PCI Express Clock: 100MHz differential clock signals.

PCIE_CLKREQA#, PCIE_CLKREQB#

Type: Input, 3.3 volt, internal Pull-Up

PCI Express Clock Request: Output enable for PCIExpress clocks

SDVO

All SDVO signals are AC-coupled. The serial capacitors are included on the module.

The following SDVO signals are located on the CoreExpress connector:

SDVOB_RED, SDVOB_RED#

Type: differential output, AC coupled

Serial Digital Video Channel B Red: SDVOB_RED is a differential data pair that provides red pixel data for the SDVOB channel during active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK signal pair.

SDVOB_GREEN, SDVOB_GREEN#

Type: differential output, AC coupled

Serial Digital Video Channel B Green: SDVOB_GREEN is a differential data pair that provides green pixel data for the SDVOB channel during active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK signal pair.

SDVOB_BLUE, SDVOB_BLUE#

Type: differential output, AC coupled

Serial Digital Video Channel B Blue: SDVOB_BLUE is a differential data pair that provides blue pixel data for the SDVOB channel during active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK signal pair.

SDVOB_CLK, SDVOB_CLK#

Type: differential output, AC coupled

Serial Digital Video Channel B Clock: This differential clock signal pair is generated by the System controller Hub internal PLL and runs between 100MHz and 200MHz.If TV-out mode is used, the SDVO_TVCLKIN clock input is used as the frequency reference for the PLL. The SDVOB_CLK output pair is then driven back to the SDVO device.

SDVOB_INT, SDVOB_INT#

Type: differential input, AC coupled

Serial Digital Video Input Interrupt: Differential input pair that may be used as an interrupt notification from the SDVO device to the System Controller Hub. This signal pair can be used to monitor hot plug attach/detach notifications for a monitor driven by an SDVO device.

SDVO_TVCLKIN, SDVO_TVCLK#

Type: differential input, AC coupled

Serial Digital Video TV-Out Synchronization Clock: Differential clock pair that is driven by the SDVO device to the System Controller Hub. If SDVO_TVCLKIN is used, it becomes the frequency reference for the system controller hub dot clock PLL, but will be driven back to the SDVO device through the SDVOB_CLK differential pair. This signal pair has an operating range of 100 —200MHz, so if the desired display frequency is less than 100MHz, the SDVO device must apply a multiplier to get the SDVO_TVCLKIN frequency into the 100- to 200-MHz range.

SDVO_STALL, SDVO_STALL#

Type: differential input, AC coupled

Serial Digital Video Field Stall: Differential input pair that allows a scaling SDVO device to stall the System Controller Hub pixel pipeline.

SDVO_CTRLCLK

Type: input/output, CMOS 3.3 volt, internal PullUp

SDVO Control Clock: Single-ended control clock line from the System Controller Hub to the SDVO device. Similar to I^2C clock functionality, but may run at faster frequencies. SDVO_CTRLCLK is used in conjunction with SDVO_CTRLDATA to transfer device config, PROM, and monitor DDC information. This interface directly connects the system controller hub to the SDVO device.

SDVO_CTRLDATA

Type: input/output, CMOS 3.3 volt, internal PullUp

SDVO Control Data: SDVO_CTRLDATA is used in conjunction with SDVO_CTRLCLK to transfer device config, PROM, and monitor DDC information. This interface directly connects the System Controller Hub to the SDVO device.

LVDS

The LVDS data and clock signals are Low Voltage Differential Signal buffers. These signals should drive across a 100-Ohm resistor at the receiver when driving.

The following LVDS signals are located on the CoreExpress connector:

LA_DATAp[3:0]
LA_DATAn[3:0]

Type: differential output, low voltage

Channel A Differential Data Output: Differential signal pair.

LA_CLKp
LA_CLKn

Type: differential output, low voltage

Channel A Differential Clock Output: Differential signal pair.

L_DDC_CLK

Type: input/output, CMOS 3.3 volt

Display Data Channel Clock: I2C-based control signal (Clock) for EDID control

L_DDC_DATA

Type: input/output, CMOS 3.3 volt

Display Data Channel Data: I2C-based control signal (Data) for EDID control

L_CTLB_CLK

Type: input/output, CMOS 3.3 volt

Control B Clock: Can be used to control external clock chip for SSC – optional

L_CTLB_DATA

Type: input/output, CMOS 3.3 volt

Control B Data: Can be used to control external clock chip for SSC – optional

Backlight

The following signals for backlight control are located on the CoreExpress connector:

L_VDDEN

Type: output, CMOS 3.3 volt

LCD Power Enable: Panel power enable control.

L_BKLTEN

Type: output, CMOS 3.3 volt

LCD Backlight Enable: Panel backlight enable control.

L_BKLTCTL

Type: output, CMOS 3.3 volt

LCD Backlight Control: This signal allows control of LCD brightness.

PATA Port

An EIDE (**E**nhanced **I**ntegrated **D**rive **E**lectronics) port is provided by the chipset to connect up to two drives that integrate the controller (hard disk, CD-ROM etc.). To enhance the performance, this port supports Ultra DMA-100 type of transfer. The EIDE port is available on the CoreExpress connector.

The following EIDE signals are located on the CoreExpress connector:

IDE_PDD[15:0]

Type: input/output, CMOS 3.3 volt, 5 volt tolerant

Device Data: These signals drive the corresponding signals on the PATA connector. There is an internal 13.3-kΩ pull-down on PATA_DD7.

IDE_PDA[2:0]

Type: output, CMOS 3.3 volt, 5 volt tolerant

Device Address: These output signals are connected to the corresponding signals on the PATA connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.

IDE_PIOR#

Type: output, CMOS 3.3 volt, 5 volt tolerant

Disk I/O Read (PIO and Non-Ultra DMA): This is the command to the PATA device that it may drive data onto the DD lines. Data is latched by the System Controller Hub on the deassertion edge of PATA_DIOR#. The PATA device is selected either by the ATA register file chip selects (PATA_DCS1# or PATA_DCS3#) and the PATA_DA lines, or the PATA DMA acknowledge (PATA_DDAK#).

IDE_PDIOW#

Type: output, CMOS 3.3 volt, 5 volt tolerant

Disk I/O Write (PIO and Non-Ultra DMA): This is the command to the PATA device that it may latch data from the PATA_DD lines. Data is latched by the PATA device on the deassertion edge of PATA_DIOW#. The PATA device is selected either by the ATA register file chip selects (PATA_DCS1# or PATA_DCS3#) and the PATA_DA lines, or the PATA DMA acknowledge (PATA_DDAK#).

IDE_PDDACK#

Type: output, CMOS 3.3 volt, 5 volt tolerant

Device DMA Acknowledge: This signal directly drives the DAK# signals on the PATA connectors. Each is asserted by the System Controller Hub to indicate to PATA DMA slave devices that a given data transfer cycle (assertion of PATA_DIOR# or PATA_DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master PATA function and are not associated with any AT-compatible DMA channel.

IDE_PDCS3#

Type: output, CMOS 3.3 volt, 5 volt tolerant

Device Chip Select for 300 Range: This chip select is for the ATA control register block. This is connected to the corresponding signal on the connector.

IDE_PDCS1#

Type: output, CMOS 3.3 volt, 5 volt tolerant

Device Chip Selects for 100 Range: This chip select is for the ATA command register block. This is connected to the corresponding signal on the PATA connector.

IDE_PDDREQ

Type: input, CMOS 3.3 volt, 5 volt tolerant

Device DMA Request: This input signal is directly driven from the DRQ signals on the PATA connector. It is asserted by the PATA device to request a data transfer, and used in conjunction with the PCI bus master PATA function and are not associated with any AT compatible DMA channel. There is an internal 13.3kΩ pull-down on this pin.

IDE_PIORDY

Type: input, CMOS 3.3 volt, 5 volt tolerant

I/O Channel Ready (PIO): This signal will keep the strobe active (PATA_DIOR# on reads, PATA_DIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers.

INT_IRQ14

Type: input, CMOS 3.3 volt, 5 volt tolerant

IDE Interrupt: Input from the PATA device indicating request for an interrupt. Tied internally to IRQ14. CoreExpress-ECO has 10K pullup to 3.3V.

IDE_PATADET

Type: input, CMOS 3.3 volt,

Detection signal for 80-pin IDE cable. A low signal indicates the connection of a 80-pin IDE cable.

USB Ports

All data signals of the eight USB 2.0 ports are located on the on the CoreExpress connector. They are counted from USB_A to USB_H with their positive (p) and negative (n) Data lines. The port USB_C can also work as USB client. The over-current signals of port A/B, C/D, E/F, G/H are wired-or together on one signal each. The USB ports G/H do not support USB 1.0 or USB 1.1 devices but only USB 2.0 devices

USB_Ap, USB_An, USB_Bp, USB_Bn, USB_CAp, USB_Cn, USB_Dp, USB_Dn
USB_Ep, USB_En, USB_Fp, USB_Fn

Type: input/output, CMOS 3.3 volt

USB Port A:F Differentials: Bus Data/Address/Command Bus: These differential pairs are used to transmit data/address/command signals for ports A through F. These ports can be routed to either the EHCI controller or one of the three UHCI controllers and are capable of running at either high, full, or low speed.

USB_Gp, USB_Gn, USB_Hp, USB_Hn

Type: input/output, CMOS 3.3 volt

USB Port G;H Differentials: Bus Data/Address/Command Bus: These differential pairs are used to transmit data/address/command signals for ports G and H. These ports are routed only to the EHCI controller and should be used ONLY for in-system USB 2.0 devices. These USB ports do not support USB 1.0 or USB 1.1 devices

USB_A/B_OC#, USB_C/D_OC#, USB_E/F_OC#, USB_G/H_OC#

Type: input, CMOS 3.3 volt

Overcurrent Indicators: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. NOTE: this signals are not 5-V tolerant.

USB_C_Device

Type: input, CMOS 3.3 volt

USB Client Connect: This signal may be used in systems where USB port C is configured for client mode. This indicates connection to an external USB host has been established.

Note: If USB Client support is enabled in BIOS, then this signal is dedicated for USB Client Connect.
Low = no device connect, High = Host connected

Note: *Not all USB keyboard models are supported. If one does not work, try a different type and manufacturer.*

SDIO Port

The System Controller Hub contains an 8-bit SDIO/MMC port. The controller supports MMC4.0 and SDIO1.1 specifications. MMC 4.0 transfer rates can be up to 48 MHz and bus widths of 1, 4 or 8 bits. SDIO 1.1 supports transfer rates can be up to 24 MHz and bus widths of 1 or 4 bits.

The following SDIO signals are located on the CoreExpress connector:

SD0_DATA[7:0]

Type: output, CMOS 3.3 volt

SDIO Controller 0 Data: These signals operate in push-pull mode. The SD card includes internal pull-up resistors for all data lines. By default, after power-up, only SD0_DATA0 is used for data transfer. Wider data bus widths can be configured for data transfer.

Note: Due to a errata information from Intel the SDIO port on the CoreExpress-ECO module has a functional limitation in the usage of data bits. The CoreExpress specification defines eight data bit SD0 to SD7. On the CoreExpress-ECO module these data lines are supplied by the chipset and this SDIO port should originally support 1 bit, 4 bit or 8 bit mode. The errata from Intel describes that due to a chipset bug this port can only be used in 1 bit or 4 bit mode, only SD0 to SD3 data lines are supported.

The following pins are affected:

pin B85: SD0_DATA4
pin A86: SD0_DATA5
pin A87: SD0_DATA6
pin B81: SD0_DATA7

This pins must not be connected on custom baseboard designs.

If the customer will implement a standard SD card interface this will not be affected as a standard SD card interface is using only data lines SD0 to SD3.

SD0_CMD

Type: output, CMOS 3.3 volt

SDIO Controller 0 Command: This signal is used for card initialization and transfer of commands. It has two operating modes: open-drain for initialization mode, and push-pull for fast command transfer.

SD0_CLK

Type: output, CMOS 3.3 volt

SDIO Controller 0: With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal is generated by System Controller Hub at a maximum frequency of:24 MHz for SD and SDIO, 48 MHz for MMC.

SD0_WP

Type: input, CMOS 3.3 volt

SDIO Controller 0 Write Protect: These signal denote the state of the write-protect tab on SD cards.

SD0_CD#

Type: input, CMOS 3.3 volt

SDIO Controller 0 Card Detect: Indicates when a card is present in an external slot.

SD0_LED

Type: output, CMOS 3.3 volt

SDIO Controller 0 LED: Can be used to drive an external LED and indicate when transfers are occurring on the bus.

SD0_PWR#

Type: output, CMOS 3.3 volt

SDIO/MMC Power Enable: These pins are used to enable the power being supplied to an SDIO/MMC device.

High Definition Audio Interface

Caution The HDA audio controller does not support standard AC97 codec devices on baseboard. A baseboard design must use a ***HDA*** audio codec.

The following audio signals are located on the CoreExpress connector:

HDA_RST#

Type: output, CMOS 3.3 volt or 1.8 volt

HD Audio Reset: This signal is the reset to external Codecs

HDA_SYNC

Type: output, CMOS 3.3 volt or 1.8 volt

HD Audio Sync: This signal is an 48-kHz fixed rate sample sync to the Codec(s). It is also used to encode the stream number.

HDA_BITCLK

Type: output, CMOS 3.3 volt or 1.8 volt

HD Audio Clock (Output): This signal is a 24.000-MHz serial data clock generated by the High Definition Audio controller. This signal contains an integrated pull-down resistor so that it does not float when an High Definition Audio CODEC (or no CODEC) is connected.

HDA_SDATAOUT

Type: output, CMOS 3.3 volt or 1.8 volt

HD Audio Serial Data Out: This signal is a serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for HD Audio

HDA_SDATAIN1, HDA_SDATAIN0

Type: input, CMOS 3.3 volt or 1.8 volt

HD Audio Serial Data In: These serial inputs are single-pumped for a bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled.

HDA_DOCKEN#

Type: output, CMOS 3.3 volt or 1.8 volt

HD Audio Dock Enable: This active low signal controls the external HD Audio docking isolation logic. When deasserted, the external docking switch is in isolate mode. When asserted, the external docking switch electrically connects the HD Audio dock signals to the corresponding System Controller Hub signals.

HDA_DOCKRST#

Type: output, CMOS 3.3 volt or 1.8 volt

HD Audio Dock Reset: This signal is a dedicated reset signal for the codec(s) in the docking station. It works similar to, but independent of, the normal HDA_RST# signal.

HDA_SPEAKER

Type: output, CMOS 3.3 volt

Speaker: The SPKR signal is the output of counter 2 and is internally ANDed with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon SLPMODE, its output state is 0.

Low Pin Count Bus

The LPC controller implements a low pin count interface that supports the LPC 1.1 specification.

The following LPC signals are located on the CoreExpress connector:

LPC_AD[3:0]

Type: output, CMOS 3.3 volt

LPC Address/Data: Multiplexed Command, Address, Data

LPC_FRAME#

Type: output, CMOS 3.3 volt

LPC Frame: This signal indicates the start of an LPC/FHW cycle.

LPC_SERIRQ

Type: input/output, CMOS 3.3 volt

Serial Interrupt Request: This signal conveys the serial interrupt protocol.

LPC_CLKOUT[2:1]

Type: output, CMOS 3.3 volt

LPC Clock: These signals are the clocks driven by the Intel®SCH to LPC devices. Each clock can support up to two loads.

System Management Bus

The System Controller Hub provides an SMBus 1.0-compliant host controller. The host controller provides a mechanism for the CPU to initiate communications with SMB peripherals (slaves).

The following SMB signals are located on the CoreExpress connector:

SMB_DATA

Type: output, CMOS 3.3 volt open drain, internal Pullup

SMBus Data: This signal is the SMBus data pin.

SMB_CLK

Type: output, CMOS 3.3 volt open drain, internal Pullup

SMBus Clock: This signal is the SMBus clock pin.

SMB_ALERT#I CMOS3.3_OD

Type: input, CMOS 3.3 volt open drain, internal Pullup

SMBus Alert: This signal can be used to wake the system, generate an interrupt, or generate an SMI#.

Miscellaneous signals

The following miscellaneous signals are located on the CoreExpress connector:

External Power-Button

Type: input, CMOS 3.3 volt

The power button signal is located on the CoreExpress connector at pin PWR_BTN#. To activate the signal, PWR_BTN# must be pulled to ground. The signal has an internal Pullup. This signal does not send any ACPI event to the operating system. Instead, pulling this for 4 s will unconditionally turn off the system.

External Wake-Up Button

Type: input, CMOS 3.3 volt

The wake-up button signal is located on the CoreExpress connector at pin WAKE#. To activate the signal, WAKE# must be pulled to ground. The signal has an internal Pullup. This signal does not send any ACPI event to the operating system.

Reset-In Signal

Type: input, CMOS 3.3 volt

The RESET-IN signal is located on the CoreExpress connector at pin RST_IN#. To reset the board, RESET-IN must be pulled to GND.

Reset-Out Signal

Type: ouput, CMOS 3.3 volt

The RESET-OUT signal is located on the CoreExpress connector at pin RST_OUT#. The signal will go low on RESET cycle.

BIOS-DISABLE Signal

Type: input, CMOS 3.3 volt

The BIOS_DISABLE signal is located on the CoreExpress connector at pin BIOS_DISABLE#. If pulled to low, the onboard BIOS FWH will be disabled and an external FWH on the LPC bus can be used as BIOS source.

WDOUT Signal

Type: output, CMOS 3.3 volt

The Watchdog-Out signal is located on the CoreExpress connector at pin WDOUT. It indicates a Watchdog timeout event wit a high level. The watchdog timeout event indication is cleared on power-up and reset.

SUS_S3# Signal

Type: output, CMOS 3.3 volt

The SUS_S3# signal will remain low if the system is in sleep state (ACPI S3 mode)

SUS_S4/5# Signal

Type: output, CMOS 3.3 volt

The SUS_S4/5# signal will remain low if the system is in suspend state (ACPI S4/S5 mode)

Power-Good Signal

Type: input, CMOS 3.3 volt

The PowerGood signal is located on the CoreExpress connector at pin PWR_GOOD. The signal must be set to high to indicate that the power supplies on the baseboard are active and within their valid ranges. A 10Kohm pullup resistor to 3.3 volt is necessary if this signal is not used.

PowerSupply-on

Type: ouput, CMOS 3.3 volt

The PowerSupply-on signal is located on the CoreExpress connector at pin PS_ON. The signal will go high to switch on the external power supplies on the baseboard.

5 Design Guidelines

These guidelines should be used as design information for baseboard designs by customers.

5.1 General Routing Guidelines

Use the following general routing and placement guidelines to layout a new design.

- Single ended and most differential signals must be ground referenced. If changing reference plane is completely unavoidable (i.e. ground reference to power reference), proper placement of stitching caps can minimize the adverse effects of EMI and signal quality performance caused by reference plane change. Stitching capacitors are small-valued capacitors (1 µF or lower) that bridge the power and ground planes close to where a high-speed signal changes layers. Stitching caps provide a high frequency current return path between different reference planes. They minimize the impedance discontinuity and current loop area that crossing different reference planes created.
- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided. Minimize layer changes. Via count should include thru-hole connector as an effective via. If routing differential signals and a layer change is necessary, ensure that trace matching for either transmit or receive pair occurs within the same layer. Recommend to use vias as small as possible.
- DO NOT route high speed signal traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.
- DO NOT place stubs, test points, test vias on the route to minimize reflection on high speed signals. Utilize vias and connector pads as test points instead.
- DO NOT route high speed signal traces with tight bends. Match number of left and right turn bends if possible.
- E.g. for PCI Express it can be helpful for testability to route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Each net within a differential pair should be length matched on a segment-by segment basis at the point of discontinuity. Total length mismatch must not be more than 5 mils. Examples of segments might include breakout areas, routes running between two vias, routes between an AC coupling capacitor and a connector pin, and so forth. The points of discontinuity would either be the via, the capacitor pad, or the connector pin.
- Recommend keeping high speed signal traces like PCI Express 20 mils from any traces, vias and pads on the motherboard whenever possible.
- AC coupling capacitors for the TX lines are all placed on the module.

5.2 General Notes

- Pair-to-pair pitch is defined as the distance from the center of either trace in a differential pair to the same point of reference on an adjacent differential pair.
- Bus-to-Bus spacing mentioned in this table is the amount of space between two differential pairs.

5.3 PCI-Express

The PCI-Express interface on the CoreExpress-ECO uses differential signaling as defined by the PCI-Express specification.

- Single Ended Impedance: 55Ω ±15%
- Differential Impedance: 100Ω ±20%
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Maximum trace length: 6.1''
- Maximum via count: 4
- AC coupling capacitor value: 100nF / 0402

Length matching between the differential pairs is not needed. Place devices AC coupling caps (only at transmit lines) near device. Unused PCI-Express ports may be left unconnected.

5.4 SDVO

- Single Ended Impedance: 55Ω ±15%
- Differential Impedance: 100Ω ±20%
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Maximum total trace length: 3.2''
- Maximum via count: 4
- AC coupling capacitor value: 100nF / 0402

Length matching between all the differential pairs within the SDVO channel is required to be within 1” of each other. Place devices AC coupling caps (only at transmit lines) near device.

5.5 SDIO

- total maximum trace length: 3.5''
- series resistor value: 48.7Ω / 1%

Trace length matching is not needed. Place series resistor for data and clock as near as possible to the CoreExpress-ECO connector.

5.6 LVDS

LVDS CLK and Data Signals

- Single Ended Impedance: 55Ω ±15%
- Differential Impedance: 100Ω ±20%
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Maximum trace length: 4.3''
- Maximum via count: 2

Length matching between all the differential pairs within the LVDS channel is required to be within 10 mils of each other, for the entire route to help minimize latency.

LVDS Control Bus Signals

Single ended L_DDC_CLK and L_DDC_DATA signals should be routed together with a maximum length of 8".

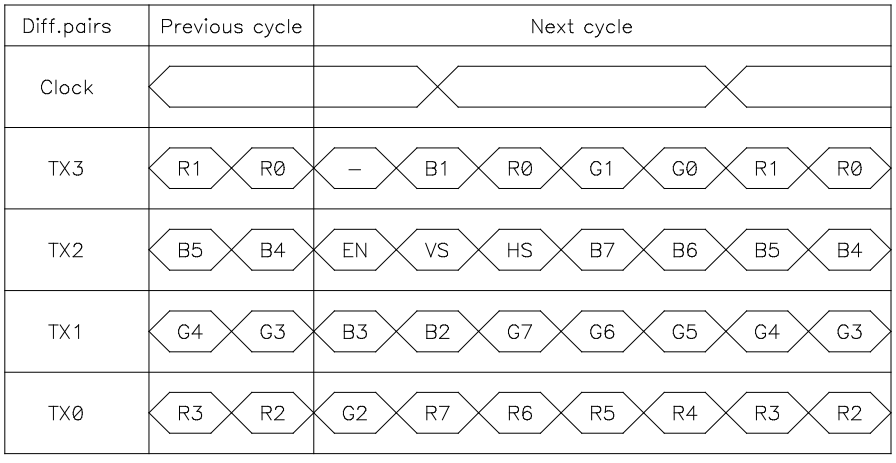
These signals have a 2.2 kΩ pull-up resistor to 3.3V on the module.

The minimum edge to edge spacing of the LVDS control bus signals (L_DDC_CLK and L_DDC_DATA) to all the other LVDS signals should be 30 mils to avoid potential noise issues. Note that this spacing requirement should be met throughout the board routes including the breakout and breakin regions.

If the control bus from the flat panel device have a different signaling voltage than 3.3 V used by the L_DDC_CLK and L_DDC_DATA signals, then a bi-directional level shifting device will be required to properly translate the voltage levels.

LVDS data timing

Example for 24bit output signals:



LVDS data mapping

	Counter	Bit Order	18 bit	24 bit
LA_DATA0	1	1	G0	G2
	2	2	R5	R7
	3	3	R4	R6
	4	4	R3	R5
	5	5	R2	R4
	6	6	R1	R3
	7	7	R0	R2
LA_DATA1	8	1	B1	B3
	9	2	B0	B2
	10	3	G5	G7
	11	4	G4	G6
	12	5	G3	G5
	13	6	G2	G4
	14	7	G1	G3
LA_DATA2	15	1	DE	DE
	16	2	VSYNC	VSYNC
	17	3	HSYNC	HSYNC
	18	4	B5	B7
	19	5	B4	B6
	20	6	B3	B5
	21	7	B2	B4
LA_DATA3	22	1		
	23	2		B1
	24	3		B0
	25	4		G1
	26	5		G0
	27	6		R1
	28	7		R0

5.7 USB 2.0

USB lines are routed directly to the CoreExpress-ECO connector. Common Mode Chokes and ESD protection diodes must be placed on the baseboard.

- Single Ended Impedance: 55Ω ±15%
- Differential Impedance: 90Ω ±15%
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Spacing to CLK signals: min. 50 mils
- Maximum trace length from CoreExpress-ECO connector to EMI choke: 8.0''
- Maximum trace length from EMI choke to ESD diode: 0.5''
- Maximum trace length from ESD diode to connector: 0.2''
- Maximum total trace length: 10.5''
- Maximum via count: 2

Length matching between the differential pairs is not needed.

5.8 PATA

- Single Ended Impedance: 55Ω ±15%

Match trace length of A/D-signals to ±500mils to strobe signals.

5.9 HD-Audio

- maximum trace length from CoreExpress-ECO connector to series resistor: 5.5''
- maximum trace length from series resistor to Audio Codec: 1.0''
- series resistor value: 33Ω / 1%

Trace length matching is not needed. Place series resistors near to the respective signal source.

5.10 SMBus

Bus capacitance must not exceed 200pF. If the bus capacitance is exceeded, then a bus bridge like the Philips PCA9515 must be used to obtain a second SMBus segment with an additional capacitance of 400pF.

Cumulate the pin capacitances of the SMBus devices and add 4pF per inch of trace length on the baseboard. The result is the bus capacitance.

5.11 LPC Bus

There are no special design rules for the LPC Bus. No series resistors are needed.

5.12 PCI IRQ Routing

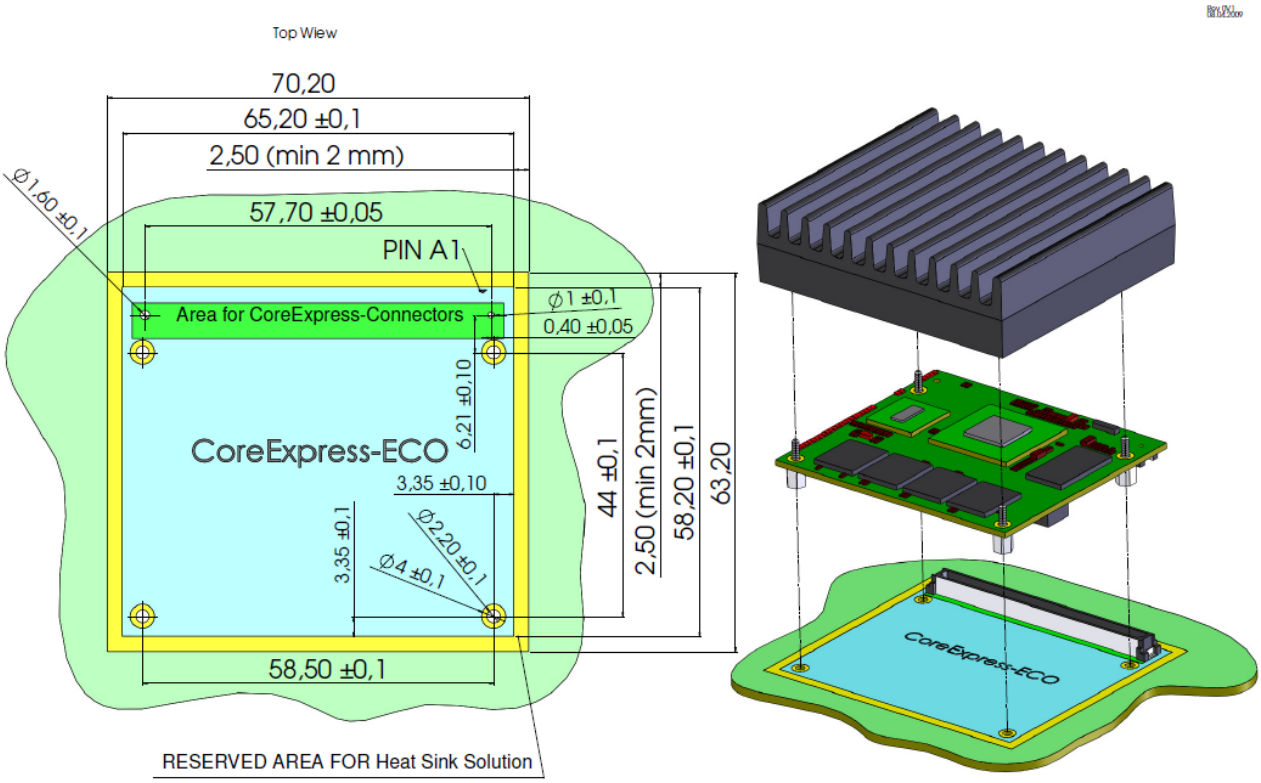
If PCI devices are implemented on a customer baseboard by using a PCI-Express to PCI bridge the PCI IRQ routing should be done according to the following table:

PCI IRQ line on bridge device	IDSEL for PCI device
INTA#	AD16
INTB#	AD17
INTC#	AD18
INTD#	AD19

This routing is supported in the standard bios of the CoreExpress-ECO.

5.13 Restricted Areas

It is required to leave an area around the CoreExpress-ECO module free of components, to accommodate the heatsink. In order to achieve good EMC characteristics, the yellow area shown in the figure below shall be laid out as a non-insulated copper frame, which is connected to ground (GND).



6 Using the Module

6.1 BIOS

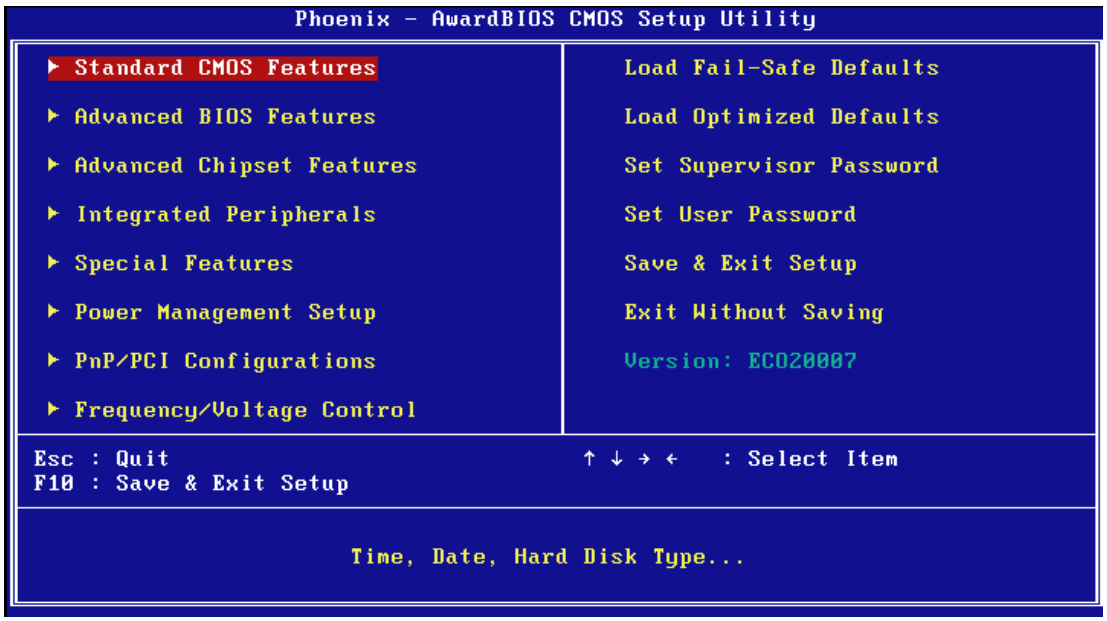
The CoreExpress-ECO module is delivered with a standard BIOS. The default setting guarantees a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in a flash prom and can be easily updated on board with software under DOS.

All changes in the setup of the BIOS are stored in the CMOS RAM of the real time clock. A copy of the CMOS RAM excluding date and time data is stored in the flash ROM. This means that even if the backup battery runs out of power, the CMOS settings are not lost. Only date and time will be set to their default value. To keep date and time alive the board must be powered with a battery voltage 2.5 to 3.6 volts at the pin BAT_IN of the CoreExpress connector.

Setup

Pressing <**F2**> or <**DEL**> at power-up starts the setup utility.

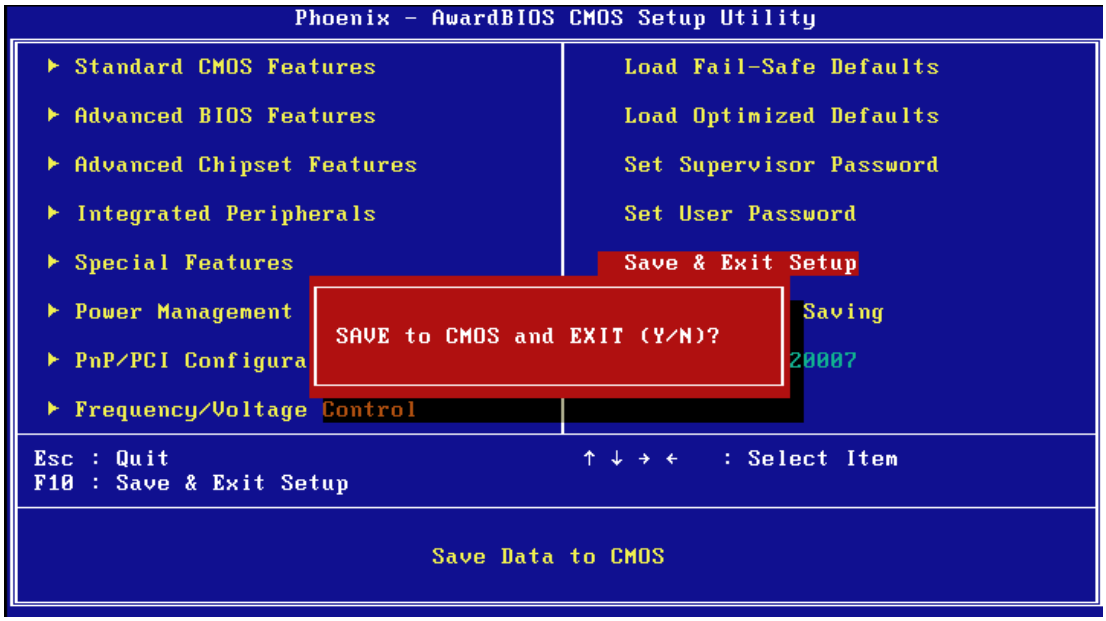


Initialize BIOS at first startup

It is important to initialize the BIOS setting at first startup of the board.

The "Optimized Defaults" is the optimized BIOS setup for the CoreExpress-ECO.

Call setup by pressing <**F2**> or <**DEL**> at power-up and executed **Load Optimized Defaults**. Then use **Save & Exit Setup** to save and activate the new settings.



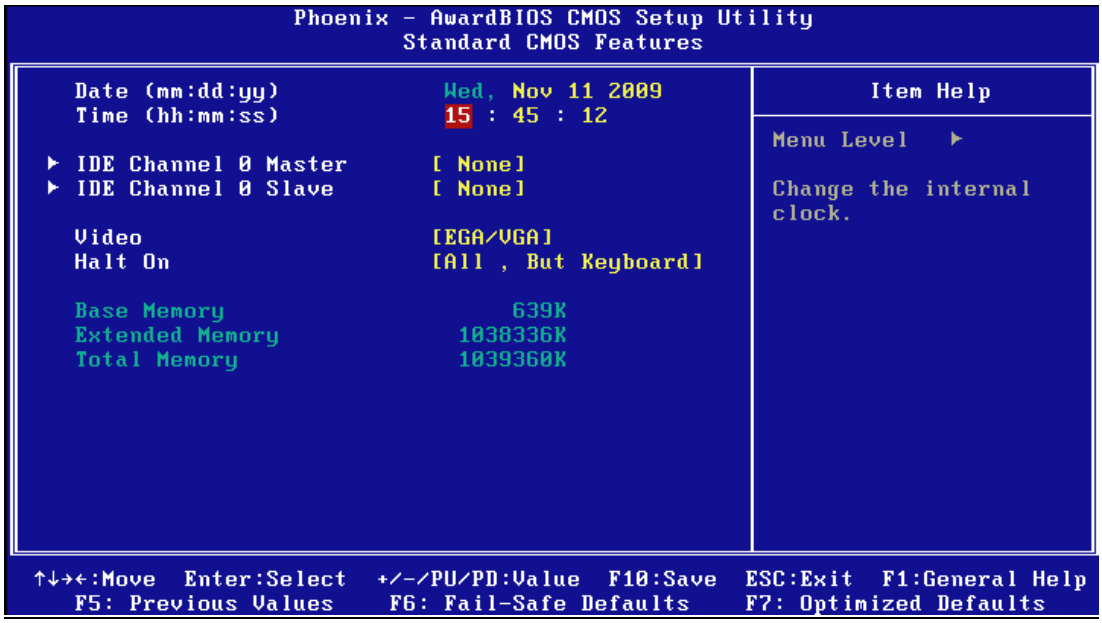
Booting from alternative device

Pressing the <**ESC**> key at power-up starts the Boot Menu. Choose one of the listed bootable devices for booting.

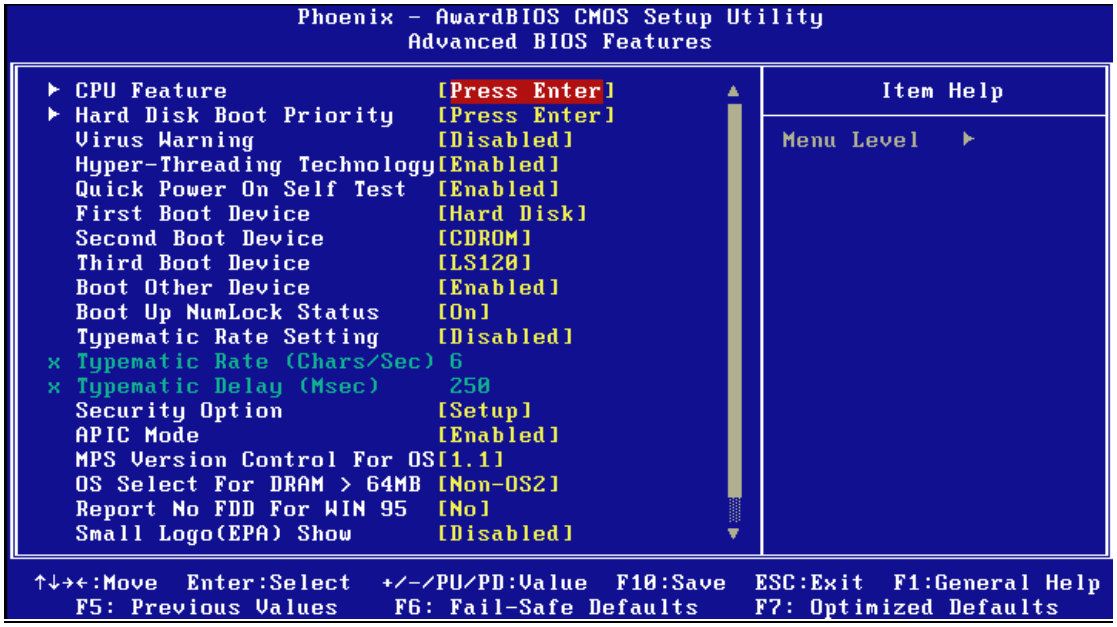
BIOS Screens

The BIOS setup utility allows setting of various board parameters. The following pictures show the different setup menus. The Cool RoadRunner-PM specific settings are explained here.

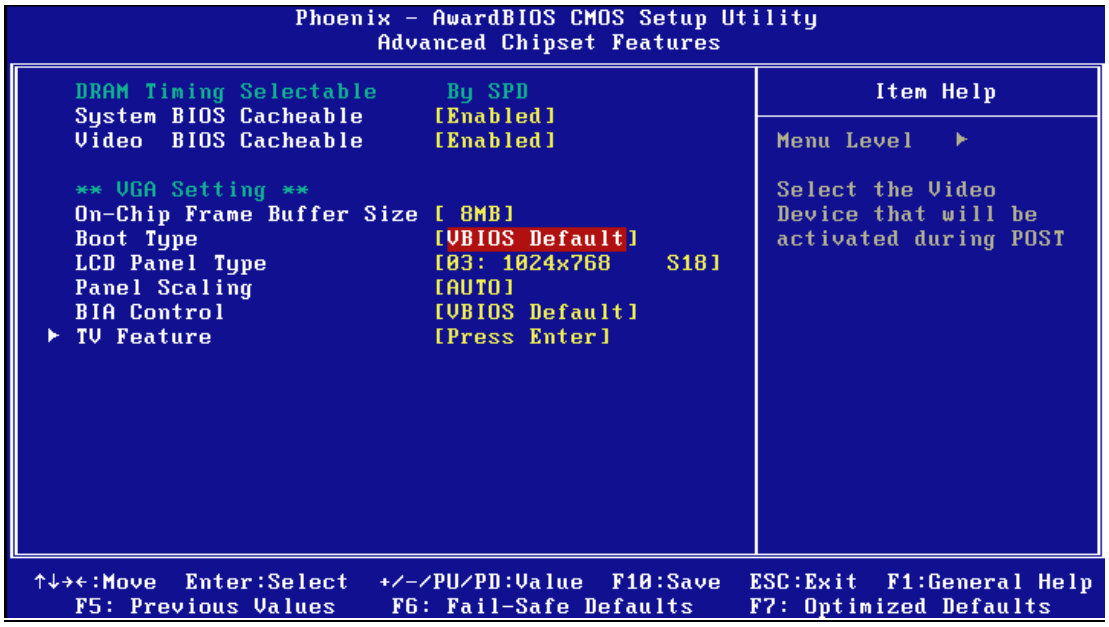
Standard CMOS Features



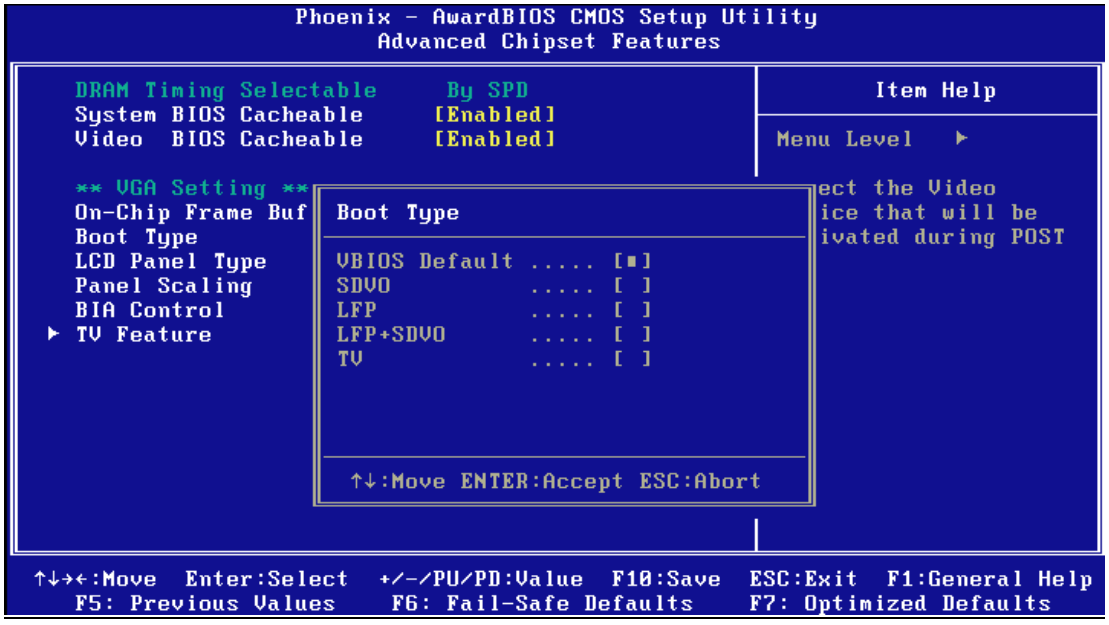
Advanced BIOS Features



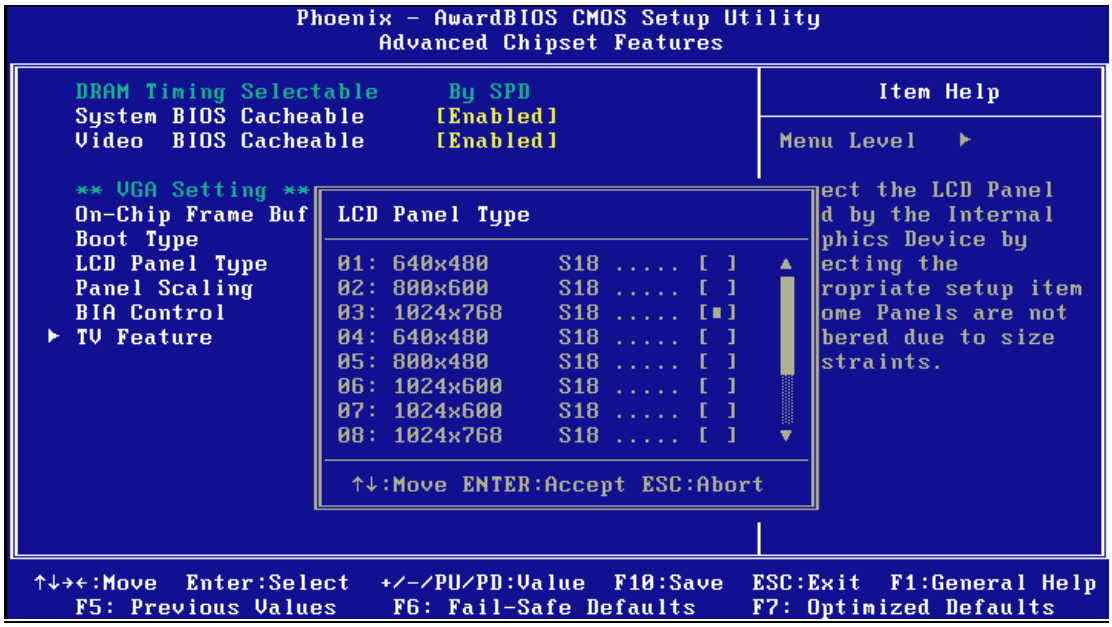
Advanced Chipset Features



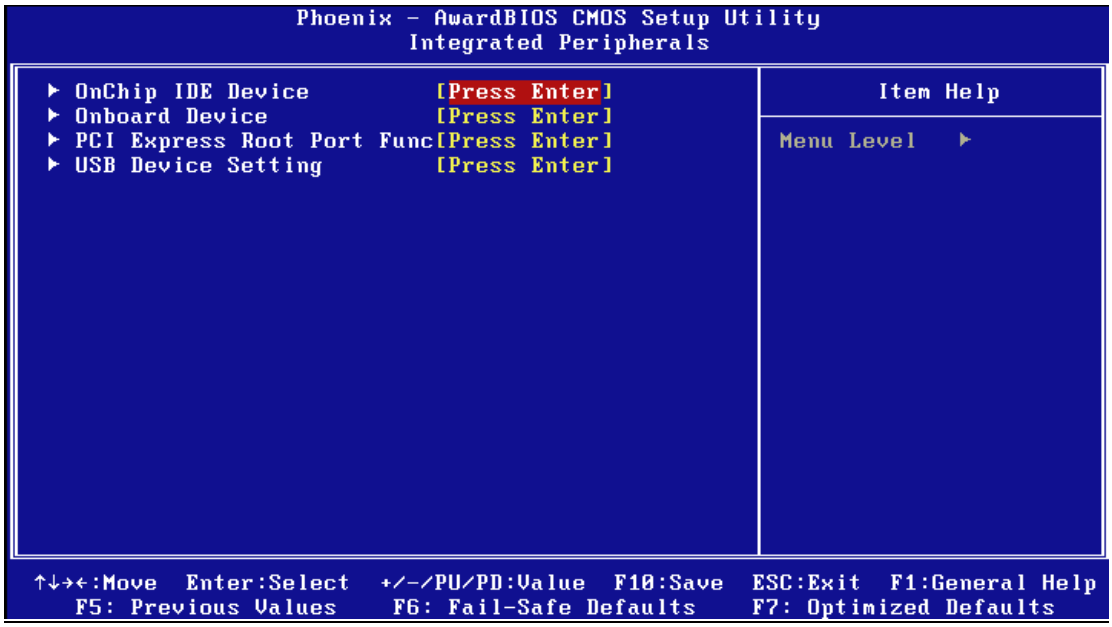
Advanced Chipset Features, Boot Type



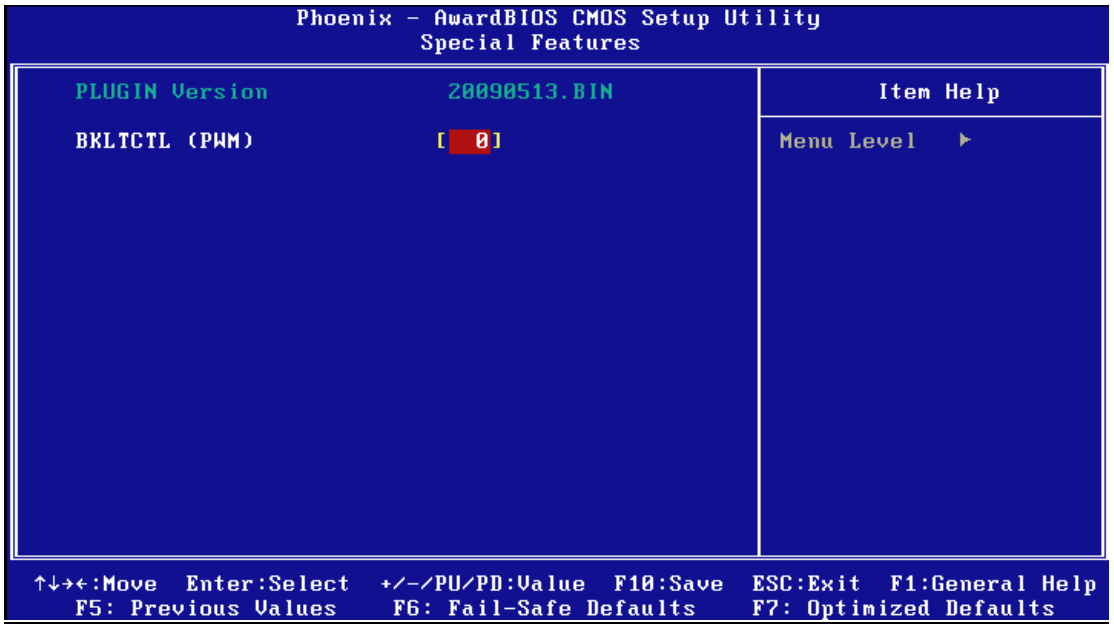
Advanced Chipset Features, LCD Panel Type



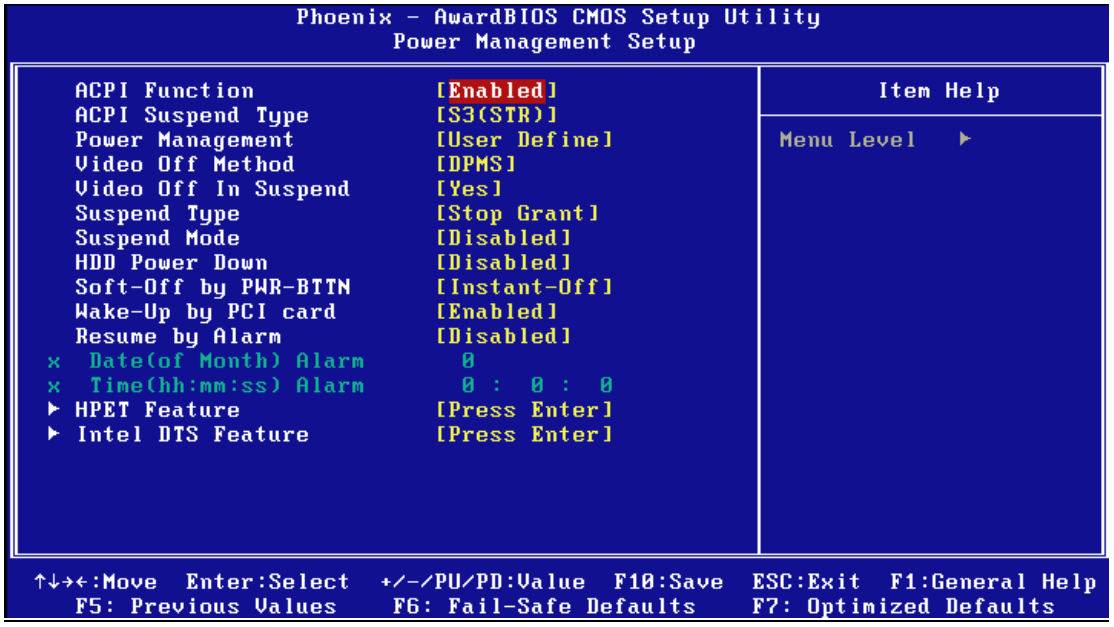
Integrated Peripherals



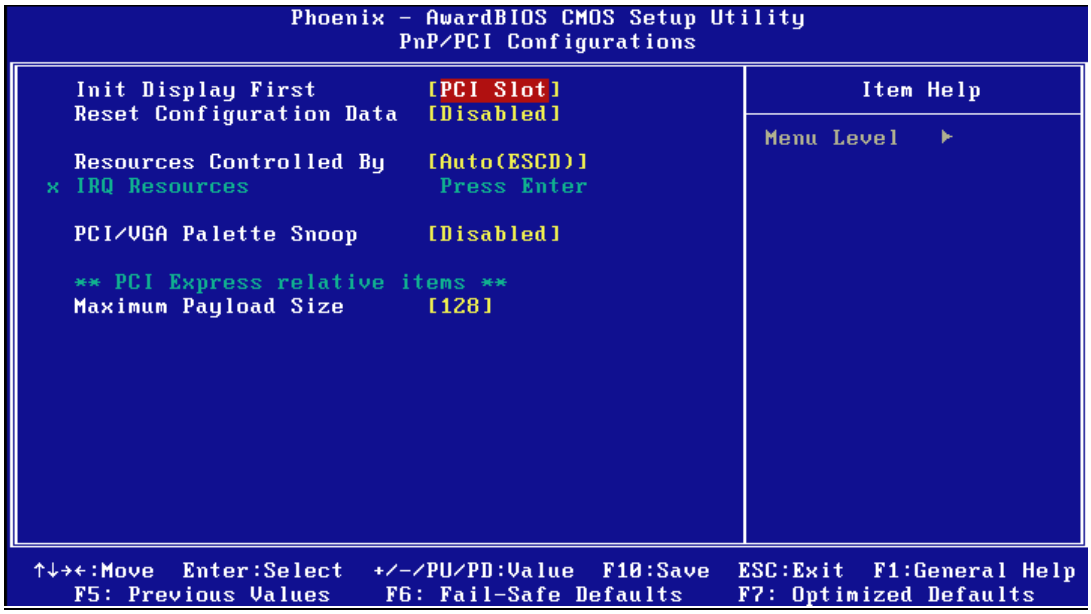
Special Features



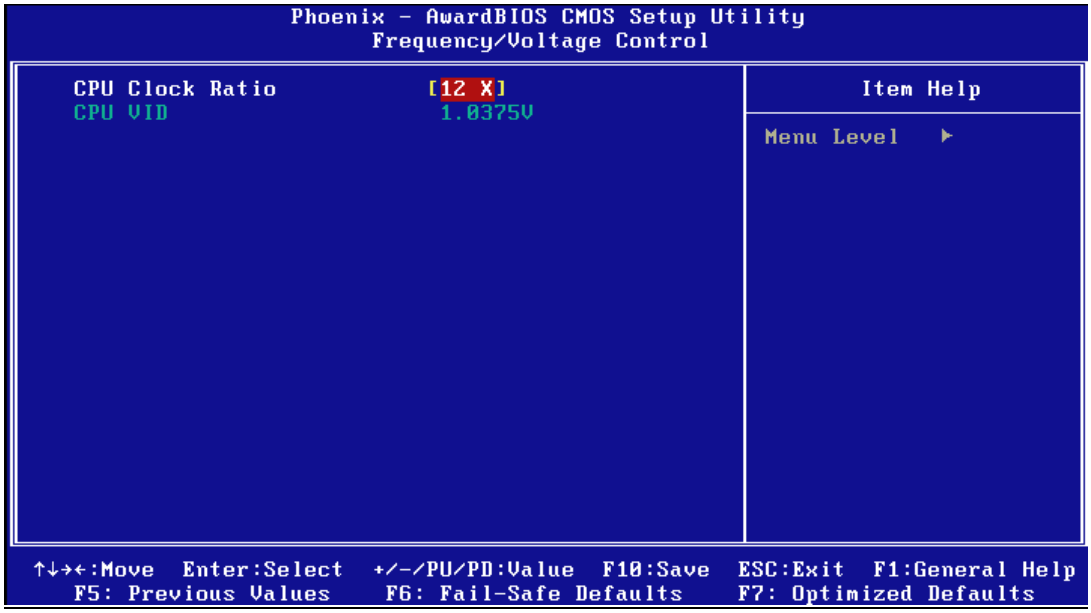
Power Management Setup



PnP/PCI Configurations



Frequency/Voltage Control



6.2 Drivers

There are drivers for different operating systems available.

Please contact our support team at **support@lippertembedded.com** to inquire the availability of the drivers.

Follow the installation instructions that come with the drivers.

7 Address Maps

This section describes the layout of the CPU memory and I/O address spaces.

Note *Depending on enabled or disabled functions in the BIOS, other or more resources may be used*

7.1 Memory Address Map

The system occupies the following memory below 1 MByte.

Address Range		Address Range (Hex)			Size	Description
896K	- 1024K	E0000	-	FFFFF	128K	System BIOS
832K	- 895K	D0000	-	DFFFF	64K	PCI Bus
768K	- 832K	C0000	-	CFFFF	64K	Graphics BIOS
704K	- 767K	B0000	-	BFFFF	64K	VGA Memory
640K	- 704K	A0000	-	AFFFF	64K	VGA Memory
0K	- 640K	0	-	9FFFF	640K	Conventional Memory

7.2 I/O Address Map

The system chip set implements a number of registers in I/O address space. These registers occupy the following map in the I/O space.

Register Address	Size	Description
0000 – 000F	16 bytes	DMA Controller 1 (8237)
0020 – 0021	2 bytes	Interrupt Controller 1 (8259)
0040 – 005F	4 bytes	Timer Controller (8254)
0040 – 005F	32 bytes	Timer Controller (8254)
00A0 – 00A1	2 bytes	Interrupt Controller 2 (8259)
0170 – 0177	8 bytes	IDE Controller
01F0 – 01F7	8 bytes	IDE Controller
0376	1 byte	IDE Controller
03B0 – 03BB	11 bytes	VGA Adapter
03C0 – 03DF	32 bytes	VGA Adapter
03F6	1 byte	IDE Controller
2000-2FFF	4096 bytes	PCI-PCI bridge
2000-3FFF	4096 bytes	PCI-PCI bridge
4000-401E	29 bytes	USB Controller
4020-403E	29 bytes	USB Controller
4040-405E	29 bytes	USB Controller
4060-406E	15 bytes	IDE Controller
4070-4076	7 bytes	VGA Controller

7.3 Interrupts

IRQ	System Resource
NMI	Parity Error
0	Timer
1	Keyboard
2	Interrupt Controller 2
3	Available
4	Available
5	Available
6	Available
7	USB Controller
8	Real Time Clock
9	Available
10	PCI-PCI Bridge
11	VGA Adapter
12	Available
13	Math coprocessor
14	EIDE
15	Available

Note Depending on the BIOS settings, it's possible to reserve several IRQ's for the PCI bus

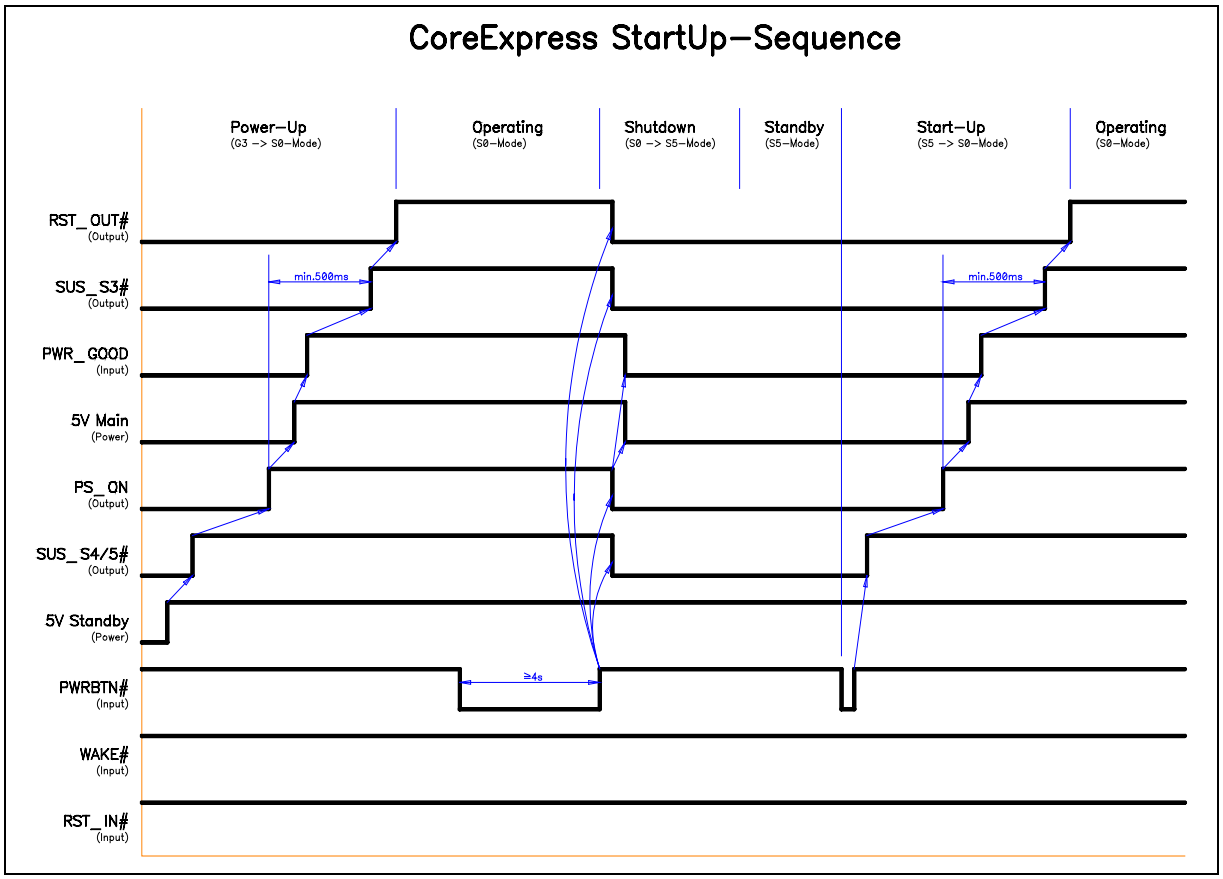
7.4 DMA Channels

DMA	Data width	System Resource
0	8 bits	Available
1	8 bits	Available
2	8 bits	Available
3	8 bits	Available
4		Reserved, Cascade Channel
5	16 bits	IDE Controller
6	16 bits	Available
7	16 bits	Available

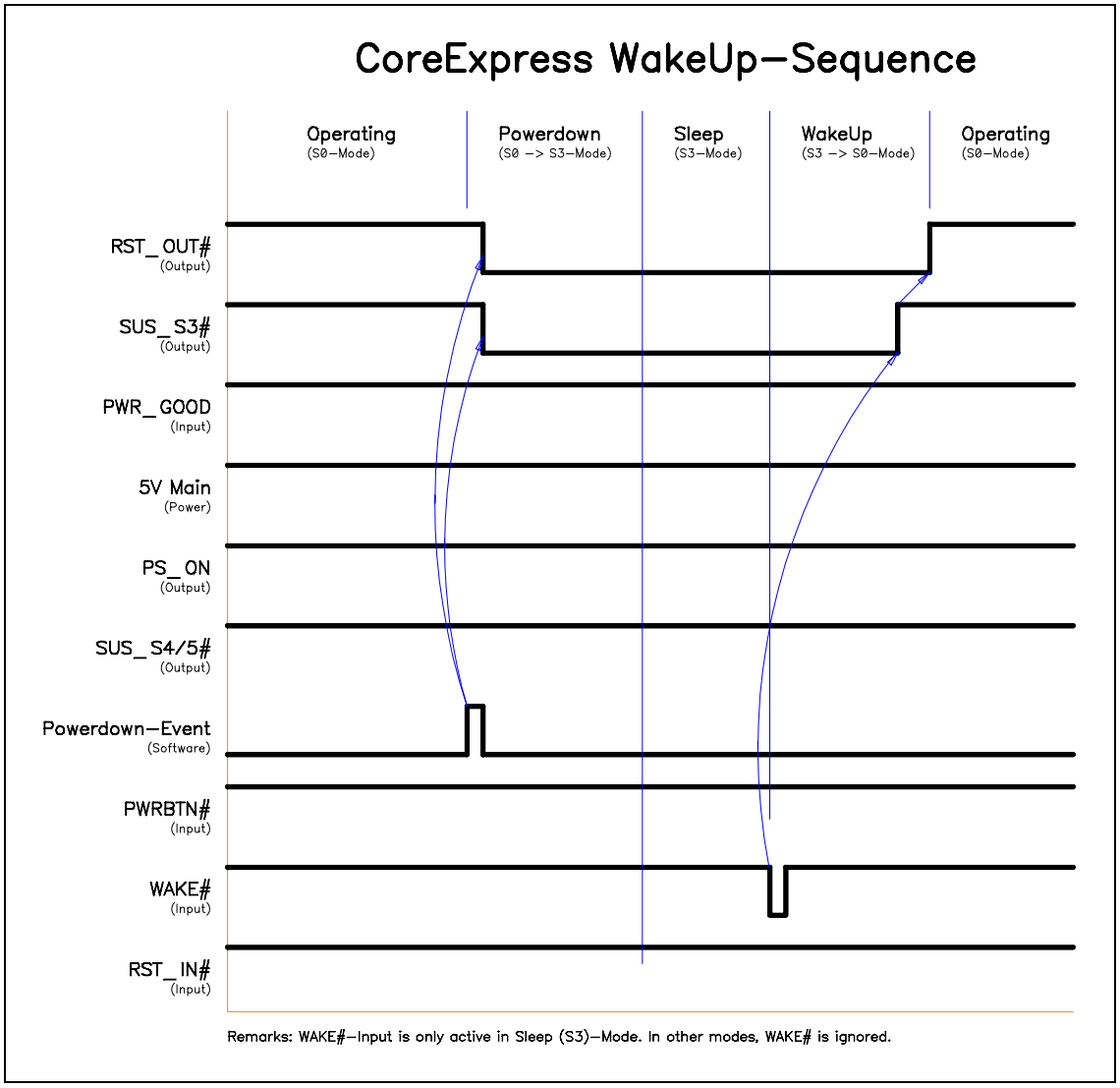
8 Timings

The following timings are for CoreExpress-ECO based on PCB rev. 407-0001-10 .

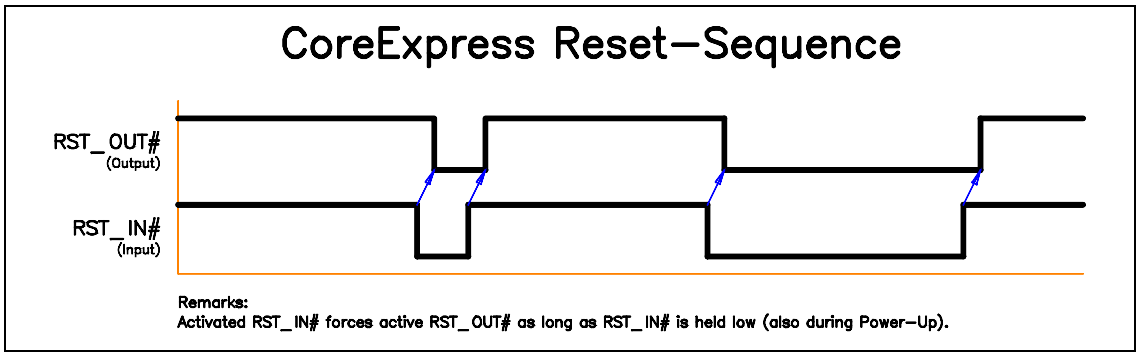
8.1 Start-Up



8.2 Wake-Up



8.3 Reset



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Getting Help

Should you have technical questions that are not covered by the respective manuals, please contact our support department at **support@lippertembedded.com**.

Please allow one working day for an answer!

Technical manuals as well as other literature for all LiPPERT products can be found in the *Products* section of LiPPERT's website www.lippertembedded.com. Simply locate the product in question and follow the link to its manual.

Returning Products for Repair

To return a product to LiPPERT for repair, you need to get a Return Material Authorization (RMA) number first.
Please fill in the RMA Request Form at http://www.lippertembedded.com/service/repairs.html and send it to us. We'll return it to you with the RMA number.

Deliveries without a valid RMA number are returned to sender at his own cost!

LiPPERT has a written Warranty and Repair Policy, which can be retrieved from
http://www.lippertembedded.com/media/downloads/General/BM14007_1V6.pdf

It describes how defective products are handled and what the related costs are. Please read this document carefully before returning a product.

Additional Information

CoreExpress

http://www.CoreExpress.com

http://www.sff-sig.org

Intel® Atom

http://www.intel.com/design/intarch/atom500/index.htm

Intel® System Controller Hub

http://www.intel.com/design/chipsets/embedded/SCHUS15W/techdocs.htm

USB

Universal Serial Bus (USB) connects computers, peripherals and more at www.usb.org

PCI-Express

PCI Express Specification, Revision 1.1 at www.pcisig.com/specifications/pciexpress/

ACPI

Advanced Configuration and Power Interface Specification (ACPI), Revision 3.0 at www.acpi.info/spec.htm

SMB

System Management Bus (SMBus) at www.smbus.org

Revision History

Filename	Date	Edited by	Change
TME-CEX-ECO-R0V0	2008-03-26	MF	Draft
TME-CEM-ECO-R0V2	2008-04-03	MF	Minor changes after review
TME-CEM-ECO-R1V0	2008-04-04	PK	Formatted and released
TME-CEM-ECO-R1V1	2008-04-05	MF	Layout guidelines updated Mechanical drawing corrected
TME-CEM-ECO-R1V2	2008-04-25	PK	Chapter 5.12 "Restricted Areas" introduced
TME-CEM-ECO-R1V3	2008-05-05	PK	Chapter 4.2: Description LPC_CLKRUN removed. Signal is not used.
TME-CEM-ECO-R1V4	2008-07-18	PK	Chapter 2.2: Change pin description to "A1"
TME-CEM-ECO-R1V5	2008-08-11	MF	Corrections in pin description
TME-CEM-ECO-R1V6	2008-10-21	MF	- Added 2 GByte Memory option, - Added power control pins and 5V standby voltage in pin description
TME-CEM-ECO-R1V7	2009-01-16	PK	- CoreExpress is Registered Trademark ® - Block diagram updated - Some editorial changes
TME-CEM-ECO-R1V8	2009-04-21	MF	- Restricted area drawing update
TME-CEM-ECO-R1V9	2009-05-07	AG	- some text corrections - SD/SDIO/MMC 4 Bit - mechanical view connector improved - MTBF updated - added chapter Timing
TME-CEM-ECO-R1V10	2009-08-25	PK	LiPPERT's phone number corrected
TME-CEM-ECO-R1V11	2009-12-08	AG	- Pullup for INT_IRQ14 on module - added LVDS data timing - added LVDS data mapping - added BIOS screenshots
TME-CEM-ECO-R1V12	2010-02-26	MF	- removed ´Confidential under NDA´ - added Inrush current - included IRQ Routing for PCI Devices on baseboards
TME-CEM-ECO-R2V0	2010-03-10 2010-04-21	MF AG	- added paragraph 1.2 about compatibility to SFF-SIG specification - Ch 4.1 added note about affected IDE pins - battery voltage range is 2.5V – 3.6V
TME-CEM-ECO-R2V1	2010-06-11	JR	- PWR_BTN, WAKE don't trigger ACPI events
TME-CEM-ECO-R2V2	2010-09-09	PK	Ch. 1.3: Article numbers corrected